4-/8-Channel 24-Bit µPower No Latency ΔΣ™ ADCs

FEATURES

- **Pin Compatible 4-/8-Channel 24-Bit ADCs**
- **Single Conversion Digital Filter Settling Time Simplifies Multiplexing**
- **4ppm INL, No Missing Codes**
- **4ppm Full-Scale Error**
- **0.5ppm Offset**
- **0.3ppm Noise**
- Internal Oscillator—No External Components Required
- 110dB Min, 50Hz/60Hz Notch Filter
- Reference Input Voltage: 0.1V to V_{CC}
- Live Zero—Extended Input Range Accommodates 12.5% Overrange and Underrange
- Single Supply 2.7V to 5.5V Operation
- Low Supply Current (200µA) and Auto Shutdown

APPLICATIONS

- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain Gauge Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control
- 6-Digit DVMs

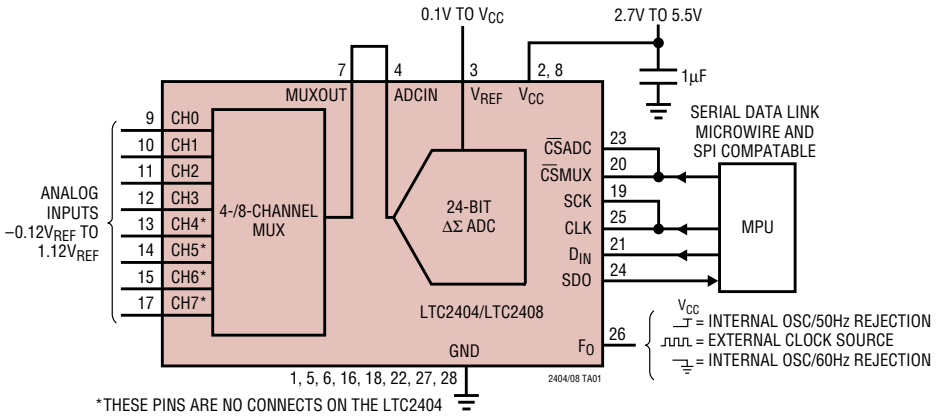
DESCRIPTION

The LTC®2404/LTC2408 are 4-/8-channel 2.7V to 5.5V micropower 24-bit A/D converters with an integrated oscillator, 4ppm INL and 0.3ppm RMS noise. They use delta-sigma technology and provide single cycle digital filter settling time (no latency delay) for multiplexed applications. The first conversion after the channel is changed is always valid. Through a single pin the LTC2404/LTC2408 can be configured for better than 110dB rejection at 50Hz or 60Hz ±2%, or can be driven by an external oscillator for a user defined rejection frequency in the range 1Hz to 120Hz. The internal oscillator requires no external frequency setting components.

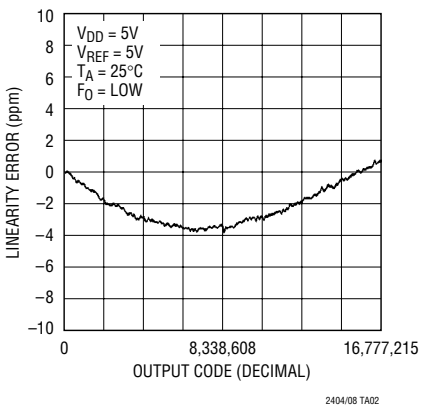
The converters accept any external reference voltage from 0.1V to V_{CC}. With their extended input conversion range of –12.5% V_{REF} to 112.5% V_{REF} the LTC2404/LTC2408 smoothly resolve the offset and overrange problems of preceding sensors or signal conditioning circuits.

The LTC2404/LTC2408 communicate through a flexible 4-wire digital interface which is compatible with SPI and MICROWIRE™ protocols.

TYPICAL APPLICATION



Total Unadjusted Error vs Output Code



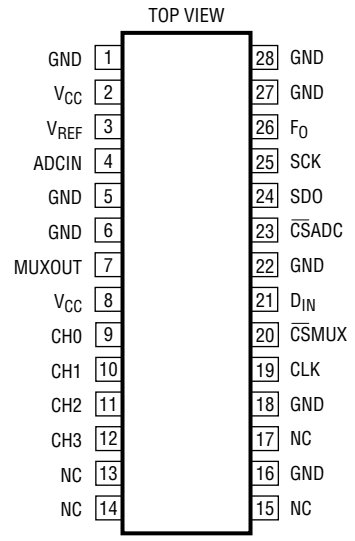
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND .....–0.3V to 7V
Analog Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)

Operating Temperature Range
LTC2404C/LTC2408C ..... 0°C to 70°C
LTC2404I/LTC2408I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

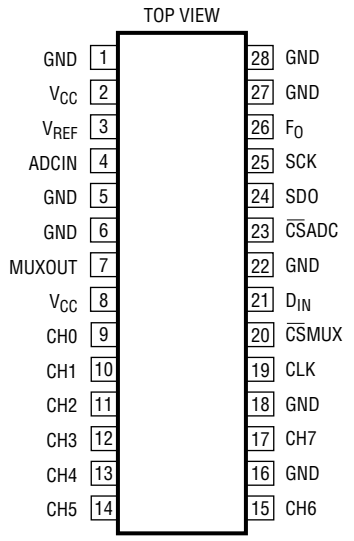


G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC2404CG
LTC2404IG



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC2408CG
LTC2408IG

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, (Note 5)	●	24			Bits
Integral Nonlinearity	V_{REF} = 2.5V (Note 6) V_{REF} = 5V (Note 6)	● ●		2 4	10 15	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}	●		0.5	2	ppm of V_{REF}
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}			0.01		ppm of V_{REF}/°C
Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}	●		4	10	ppm of V_{REF}
Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}			0.02		ppm of V_{REF}/°C
Total Unadjusted Error	V_{REF} = 2.5V V_{REF} = 5V			5 10		ppm of V_{REF} ppm of V_{REF}
Output Noise	V_{IN} = 0V (Note 13)			1.5		μV_{RMS}
Normal Mode Rejection 60Hz ±2%	(Note 7)	●	110	130		dB

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Normal Mode Rejection 50Hz ±2%	(Note 8)	●	110	130		dB
Power Supply Rejection DC	V_{REF} = 2.5V, V_{IN} = 0V			100		dB
Power Supply Rejection 60Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Note 7)			110		dB
Power Supply Rejection 50Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Note 8)			110		dB

ANALOG INPUT AND REFERENCE

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	(Note 14)	●	$-0.125 \cdot V_{REF}$		$1.125 \cdot V_{REF}$	V
V_{REF}	Reference Voltage Range		●	0.1		V_{CC}	V
$C_{S(IN)}$	Input Sampling Capacitance				10		pF
$C_{S(REF)}$	Reference Sampling Capacitance				15		pF
$I_{IN(LEAK)}$	Input Leakage Current	$\overline{CS} = V_{CC}$	●	–10	1	10	nA
$I_{REF(LEAK)}$	Reference Leakage Current	V_{REF} = 2.5V, $\overline{CS} = V_{CC}$	●	–12	1	12	nA
$I_{IN(MUX)}$	On Channel Leakage Current	V_S = 2.5V (Note 15)	●			±20	nA
R_{ON}	MUX On-Resistance	I_{OUT} = 1mA, V_{CC} = 2.7V I_{OUT} = 1mA, V_{CC} = 5V	● ●		250 120	300 250	Ω Ω
	MUX ΔR_{ON} vs Temperature				0.5		%/°C
	ΔR_{ON} vs V_S (Note 15)				20		%
$I_{S(OFF)}$	MUX Off Input Leakage	Channel Off, V_S = 2.5V	●			±20	nA
$I_{D(OFF)}$	MUX Off Output Leakage	Channel Off, V_D = 2.5V	●			±20	nA
t_{OPEN}	MUX Break-Before-Make Interval				290		ns
t_{ON}	Enable Turn-On Time	V_S = 1.5V, R_L = 3.4k, C_L = 15pF			490		ns
t_{OFF}	Enable Turn-Off Time	V_S = 1.5V, R_L = 3.4k, C_L = 15pF			190		ns
QIRR	MUX Off Isolation	$V_{IN} = 2V_{P-P}$, R_L = 1k, f = 100kHz			70		dB
QINJ	Charge Injection	R_S = 0Ω, C_L = 1000pF, V_S = 1V			±1		pC
$C_{S(OFF)}$	Input Off Capacitance (MUX)				10		pF
$C_{D(OFF)}$	Output Off Capacitance (MUX)				10		pF

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O	2.7V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 3.3V	● 	2.5 2.0			V V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V	● 			0.8 0.6	V V
V_{IH}	High Level Input Voltage SCK	2.7V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 3.3V (Note 9)	● 	2.5 2.0			V V
V_{IL}	Low Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 5.5V (Note 9)	● 			0.8 0.6	V V
I_{IN}	Digital Input Current $\overline{CS}$, F_O	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 9)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 9)			10		pF
V_{OH}	High Level Output Voltage SDO	I_O = –800µA	●	V_{CC} – 0.5V			V
V_{OL}	Low Level Output Voltage SDO	I_O = 1.6mA	●			0.4V	V
V_{OH}	High Level Output Voltage SCK	I_O = –800µA (Note 10)	●	V_{CC} – 0.5V			V
V_{OL}	Low Level Output Voltage SCK	I_O = 1.6mA (Note 10)	●			0.4V	V
I_{OZ}	High-Z Output Leakage SDO		●	–10		10	µA
V_{IN} H_{MUX}	MUX High Level Input Voltage	V^+ = 3V	●	2			V
V_{IN} L_{MUX}	MUX Low Level Input Voltage	V^+ = 2.4V	●			0.8	V

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode	 $\overline{CS}$ = 0V (Note 12) $\overline{CS}$ = V_{CC} (Note 12)	 ● ●		 200 20	 300 30	 µA µA
$I_{CC(MUX)}$	Multiplexer Supply Current	All Logic Inputs Tied Together V_{IN} = 0V or 5V	●		15	40	µA

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	2.56		307.2	kHz
t_{HEO}	External Oscillator High Period		●	0.5		390	µs
t_{LEO}	External Oscillator Low Period		●	0.5		390	µs
t_{CONV}	Conversion Time	F_O = 0V F_O = V_{CC} External Oscillator (Note 11)	● ● ●	130.66 156.80 20480/f_{EOSC} (in kHz)	133.33 160	136 163.20	ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)			19.2 f_{EOSC}/8		kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)		45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 9)	●			2000	kHz
t_{LESCK}	External SCK Low Period	(Note 9)	●	250			ns
t_{HESCK}	External SCK High Period	(Note 9)	●	250			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	● ●	1.64 256/f_{EOSC} (in kHz)	1.67	1.70	ms ms
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 9)	●	32/f_{ESCK} (in kHz)			ms
t_1	$\overline{CS}$ ↓ to SDO Low Z		●	0		150	ns
t_2	$\overline{CS}$ ↑ to SDO High Z		●	0		150	ns
t_3	$\overline{CS}$ ↓ to SCK ↓	(Note 10)	●	0		150	ns
t_4	$\overline{CS}$ ↓ to SCK ↑	(Note 9)	●	50			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7 to 5.5V unless otherwise specified, source input is 0Ω.

Note 4: Internal Conversion Clock source with the F_O pin tied to GND or to V_{CC} or to external conversion clock source with f_{EOSC} = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: F_O = 0V (internal oscillator) or f_{EOSC} = 153600Hz ±2% (external oscillator).

Note 8: F_O = V_{CC} (internal oscillator) or f_{EOSC} = 128000Hz ±2% (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in kHz.

Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance C_{LOAD} = 20pF.

Note 11: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses the internal oscillator. F_O = 0V or F_O = V_{CC}.

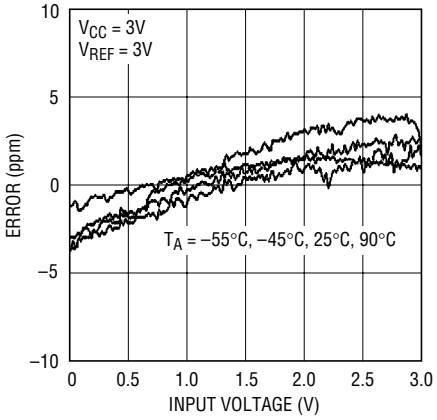
Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: For reference voltage values V_{REF} > 2.5V the extended input of $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$ is limited by the absolute maximum rating of the Analog Input Voltage pin (Pin 3). For 2.5V < $V_{REF} \leq$ $0.267V + 0.89 \cdot V_{CC}$ the input voltage range is –0.3V to $1.125 \cdot V_{REF}$. For $0.267V + 0.89 \cdot V_{CC} < V_{REF} \leq V_{CC}$ the input voltage range is –0.3V to V_{CC} + 0.3V.

Note 15: V_S is the voltage applied to a channel input. V_D is the voltage applied to the MUX output.

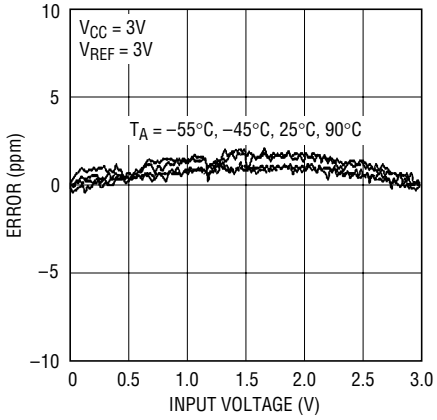
TYPICAL PERFORMANCE CHARACTERISTICS

Total Unadjusted Error (3V Supply)



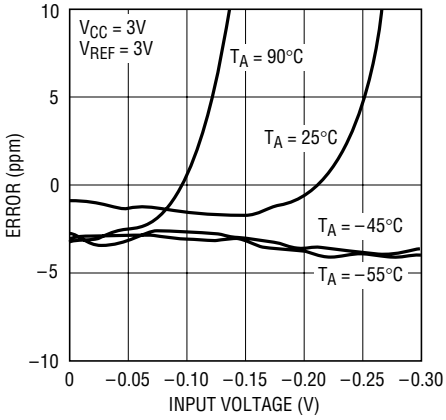
24048 G01

INL (3V Supply)



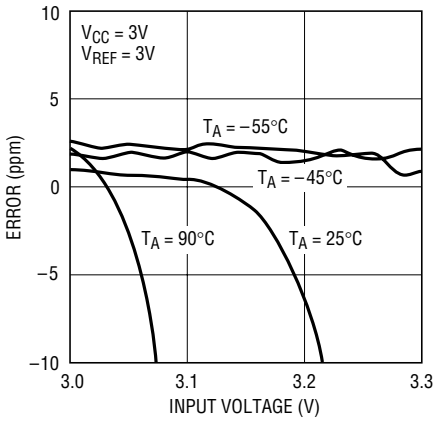
24048 G02

Negative Extended Input Range Total Unadjusted Error (3V Supply)



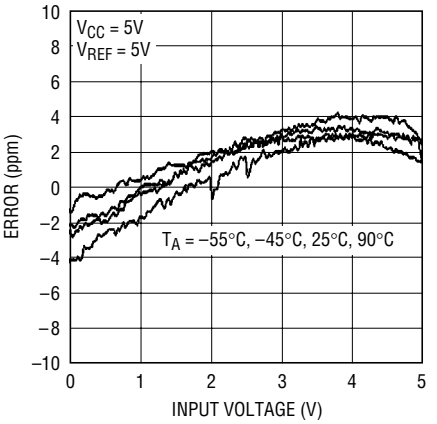
24048 G03

Positive Extended Input Range Total Unadjusted Error (3V Supply)



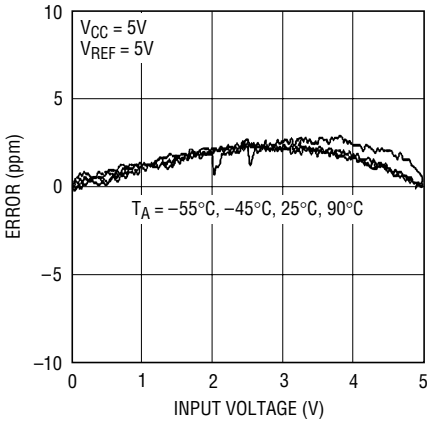
24048 G04

Total Unadjusted Error (5V Supply)



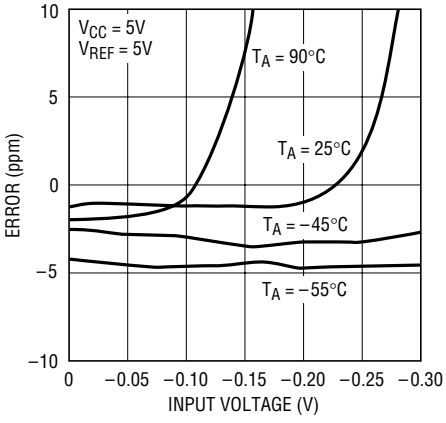
24048 G05

INL (5V Supply)



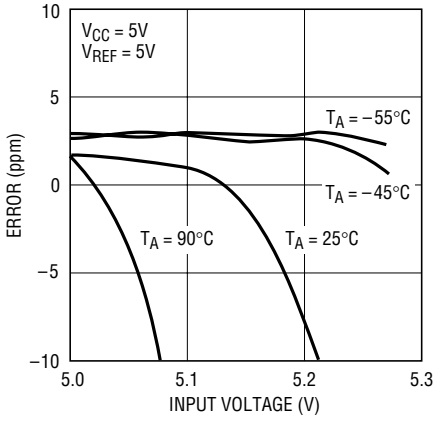
24048 G06

Negative Extended Input Range Total Unadjusted Error (5V Supply)



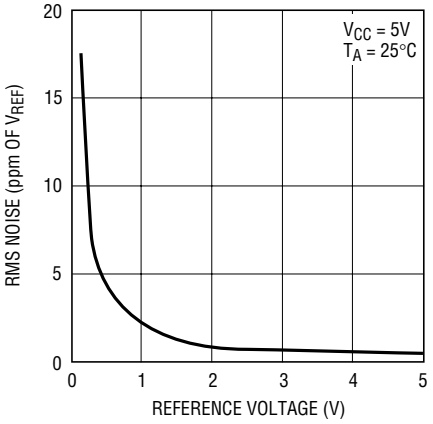
24048 G07

Positive Extended Input Range Total Unadjusted Error (5V Supply)



24048 G08

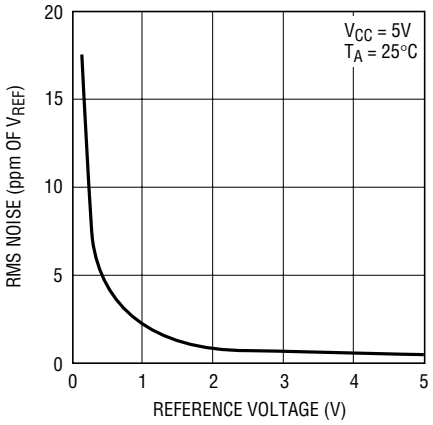
Offset Error vs Reference Voltage



24048 G10

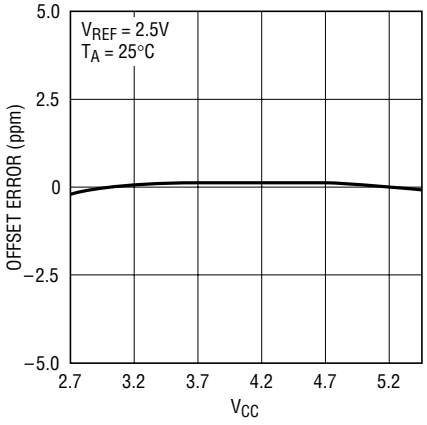
TYPICAL PERFORMANCE CHARACTERISTICS

RMS Noise vs Reference Voltage



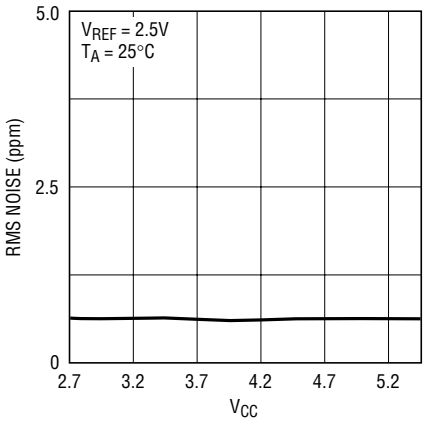
24048 G10

Offset Error vs V_{CC}



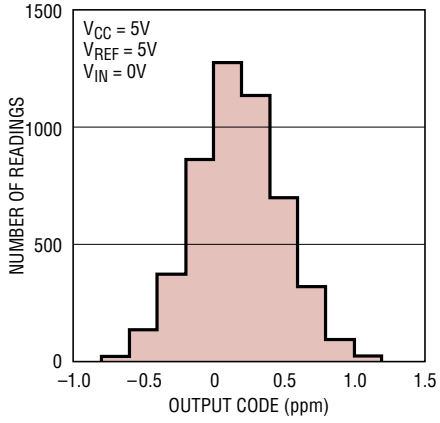
24048 G11

RMS Noise vs V_{CC}



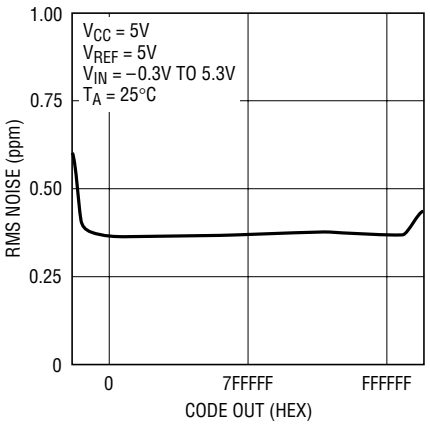
24048 G12

Noise Histogram



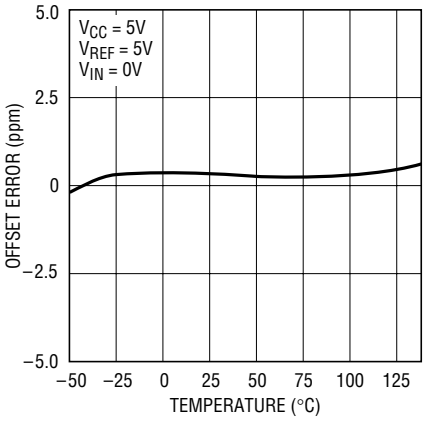
24048 G13

RMS Noise vs CODE OUT



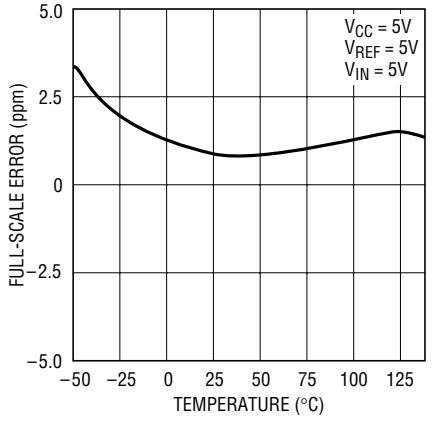
24048 G14

Offset Error vs Temperature



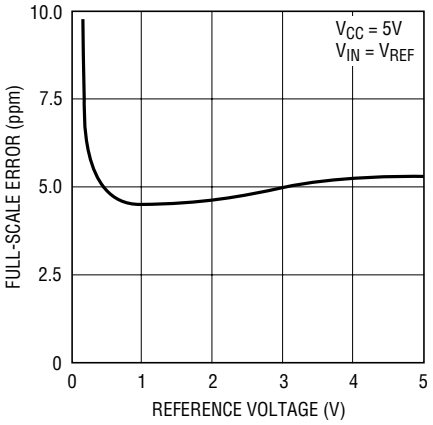
24048 G15

Full-Scale Error vs Temperature



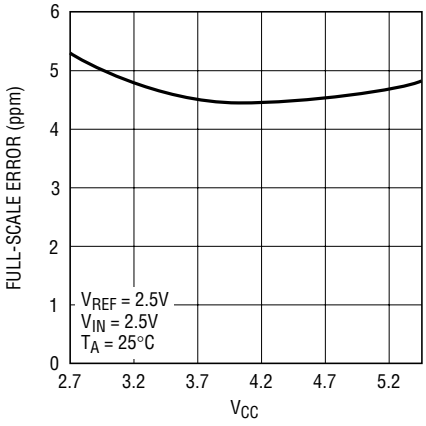
24048 G16

Full-Scale Error vs Reference Voltage



24048 G17

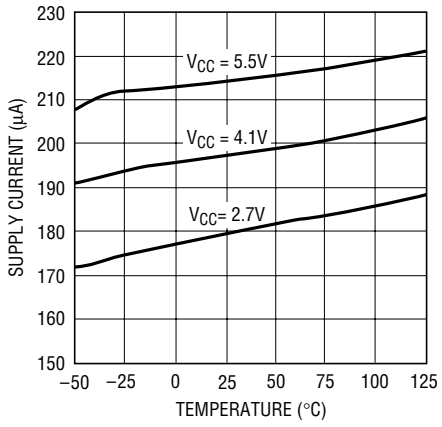
Full-Scale Error vs V_{CC}



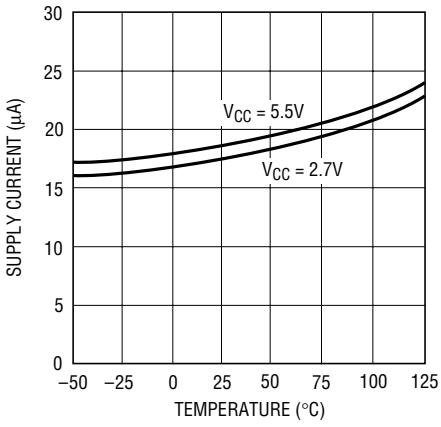
24048 G18

TYPICAL PERFORMANCE CHARACTERISTICS

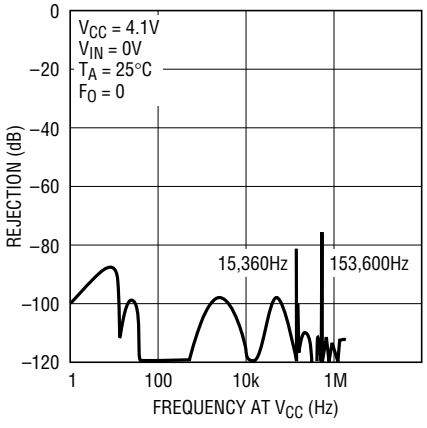
Conversion Current vs Temperature



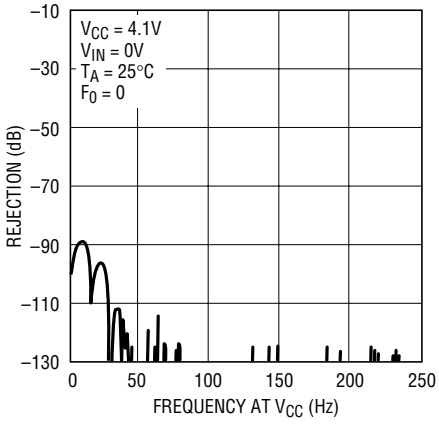
Sleep Current vs Temperature



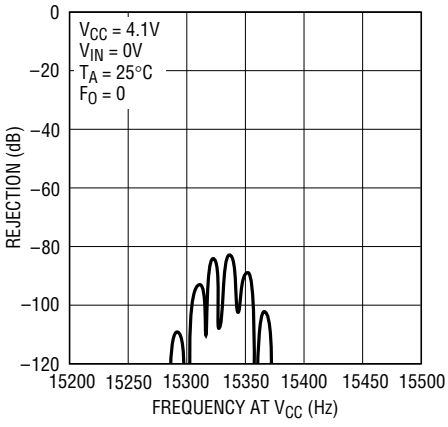
PSRR vs Frequency at V_{CC}



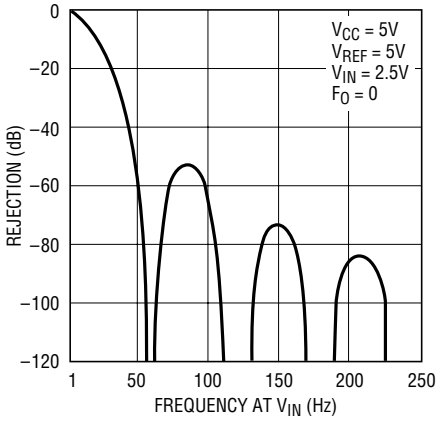
PSRR vs Frequency at V_{CC}



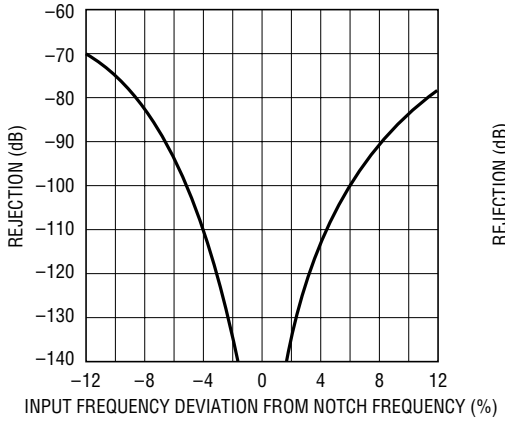
PSRR vs Frequency at V_{CC}



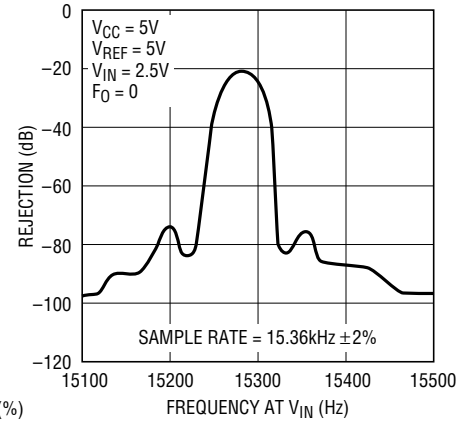
Rejection vs Frequency at V_{IN}



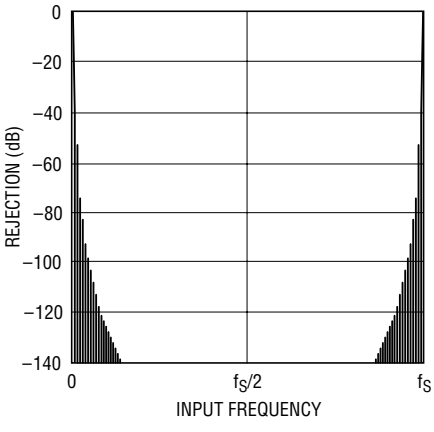
Rejection vs Frequency at V_{IN}



Rejection vs Frequency at V_{IN}

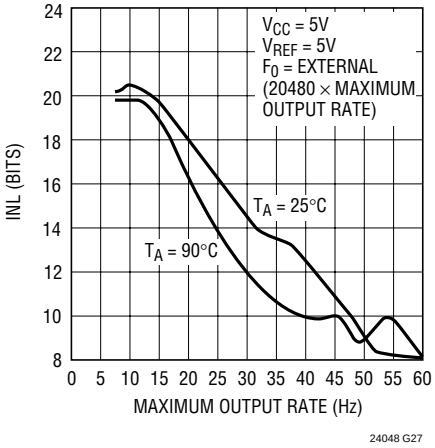


Rejection vs Frequency at V_{IN}

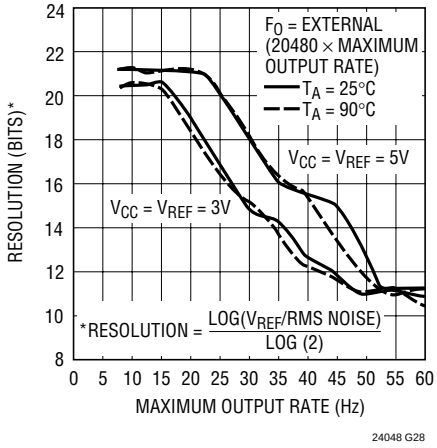


TYPICAL PERFORMANCE CHARACTERISTICS

INL vs Maximum Output Rate



Resolution vs Maximum Output Rate



PIN FUNCTIONS

GND (Pins 1, 5, 6, 16, 18, 22, 27, 28): Ground. Should be connected directly to a ground plane through a minimum length trace or it should be the single-point-ground in a single point grounding system.

V_{CC} (Pins 2, 8): Positive Supply Voltage. 2.7V ≤ V_{CC} ≤ 5.5V. Bypass to GND with a 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

V_{REF} (Pin 3): Reference Input. The reference voltage range is 0.1V to V_{CC}.

ADCIN (Pin 4): Analog Input. The input voltage range is –0.125 • V_{REF} to 1.125 • V_{REF}. For V_{REF} > 2.5V the input voltage range may be limited by the pin absolute maximum rating of –0.3V to V_{CC} + 0.3V.

MUXOUT (Pin 7): MUX Output. This pin is the output of the multiplexer. Tie to ADCIN for normal operation.

CH0 (Pin 9): Analog Multiplexer Input.

CH1 (Pin 10): Analog Multiplexer Input.

CH2 (Pin 11): Analog Multiplexer Input.

CH3 (Pin 12): Analog Multiplexer Input.

CH4 (Pin 13): Analog Multiplexer Input. No connect on the LTC2404.

CH5 (Pin 14): Analog Multiplexer Input. No connect on the LTC2404.

CH6 (Pin 15): Analog Multiplexer Input. No connect on the LTC2404.

CH7 (Pin 17): Analog Multiplexer Input. No connect on the LTC2404.

CLK (Pin 19): Shift Clock for Data In. This clock synchronizes the serial data transfer into the MUX. For normal operation, drive this pin in parallel with SCK.

$\overline{CS}$MUX (Pin 20): MUX Chip Select Input. A logic high on this input allows the MUX to receive a channel address. A logic low enables the selected MUX channel and connects it to the MUXOUT pin for A/D conversion. For normal operation, drive this pin in parallel with $\overline{CS}$ADC.

D_{IN} (Pin 21): Digital Data Input. The multiplexer address is shifted into this input on the last four rising CLK edges before $\overline{CS}$MUX goes low.

$\overline{CS}$ADC (Pin 23): ADC Chip Select Input. A low on this pin enables the SDO digital output and following each conversion, the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{CS}$ADC is high. A high on this pin also disables the SDO digital output. A low-to-high transition on $\overline{CS}$ADC during the Data Output

PIN FUNCTIONS

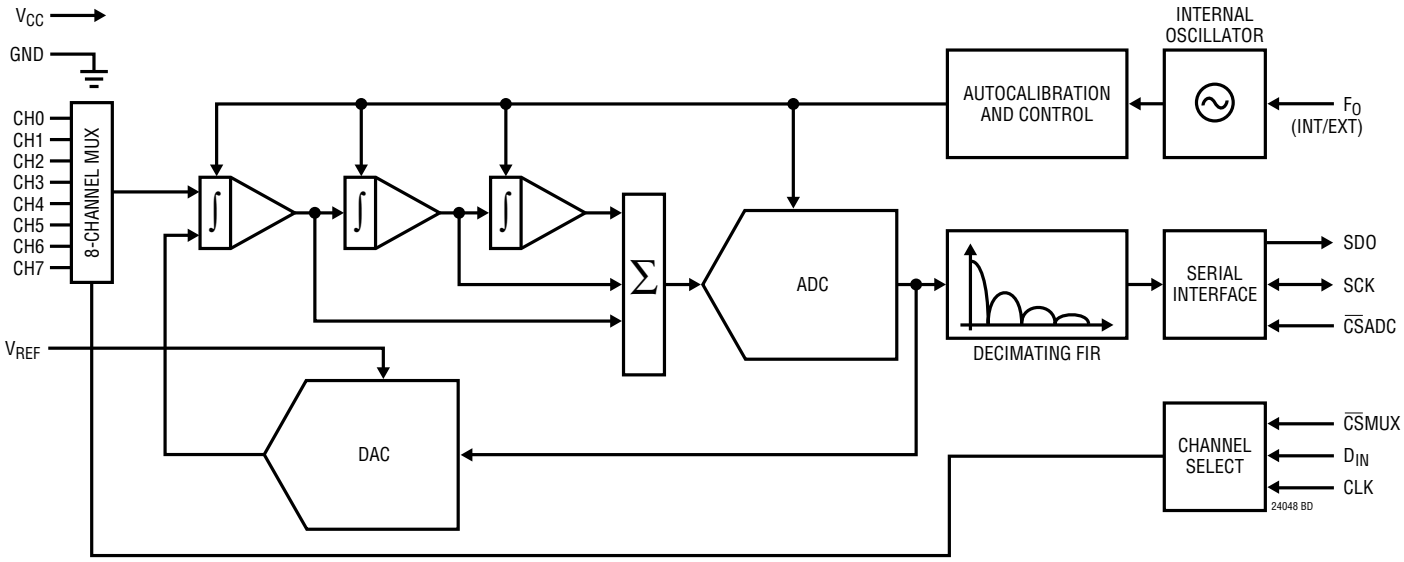
state aborts the data transfer and starts a new conversion. For normal operation, drive this pin in parallel with $\overline{CS}$MUX.

SDO (Pin 24): Three-State Digital Output. During the data output period this pin is used for serial data output. When the chip select $\overline{CS}$ADC is high ($\overline{CS}$ADC = V_{CC}), the SDO pin is in a high impedance state. During the Conversion and Sleep periods, this pin can be used as a conversion status output. The conversion status can be observed by pulling $\overline{CS}$ADC low.

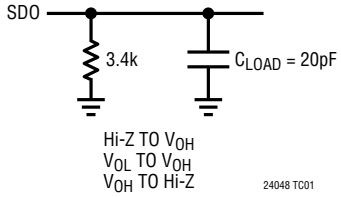
SCK (Pin 25): Shift Clock for Data Out. This clock synchronizes the serial data transfer of the ADC data output. Data is shifted out of SDO on the falling edge of SCK. For normal operation, drive this pin in parallel with CLK.

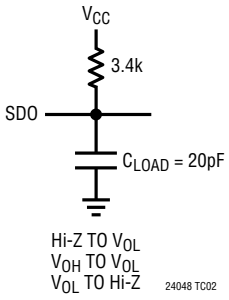
F_O (Pin 26): Digital input which controls the ADC's notch frequencies and conversion time. When the F_O pin is connected to V_{CC} ($F_O = V_{CC}$), the converter uses its internal oscillator and the digital filter first null is located at 50Hz. When the F_O pin is connected to GND (F_O = OV), the converter uses its internal oscillator and the digital filter first null is located at 60Hz. When F_O is driven by an external clock signal with a frequency f_{EOSC}, the converter uses this signal as its clock and the digital filter first null is located at a frequency $f_{EOSC}/2560$. The resulting output word rate is $f_{EOSC}/20480$.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS





APPLICATIONS INFORMATION

Converter Operation Cycle

The LTC2404/LTC2408 are low power, 4-/8-channel delta-sigma analog-to-digital converters with easy-to-use 4-wire interfaces. Their operation is simple and made up of four states. The converter operation begins with the conversion, followed by a low power sleep state and concluded with the data output (see Figure 1). Channel selection may be performed while the device is in the sleep state or at the conclusion of the data output state. The interface consists of serial data output (SDO), serial clock (CLK/SCK), chip select ($\overline{CS}$ADC/$\overline{CS}$MUX) and data input (D_{IN}). By tying SCK to CLK and $\overline{CS}$ADC to $\overline{CS}$MUX, the interface requires only four wires.

Initially, the LTC2404 or LTC2408 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in the sleep state, power consumption is reduced by an order of magnitude. The part remains in the sleep state as long as $\overline{CS}$ADC is logic HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Channel selection for the next conversion cycle is performed while the device is in the sleep state or at the end of the data output state. A specific channel is selected by applying a 4-bit serial word to the D_{IN} pin on the rising edge of CLK while $\overline{CS}$MUX is HIGH, see Figure 3 and Table 3. The channel is selected based on the last four bits clocked into the D_{IN} pin before $\overline{CS}$MUX goes low. If D_{IN} is all 0's, the previous channel remains selected.

In the example, Figure 3, the MUX channel is selected during the sleep state, just before the data output state begins. Once the channel selection is complete, the device remains in the sleep state as long as $\overline{CS}$ADC remains HIGH.

Once $\overline{CS}$ADC is pulled low, the device begins outputting the conversion result. There is no latency in the conversion result. Since there is no latency, the first conversion following a change in input channel is valid and corresponds to that channel. The data output corresponds to the conversion just performed. This result is shifted out on the serial data output pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK, see Figure 3. The data output state is concluded once 32 bits are read out of the ADC or when $\overline{CS}$ADC is brought HIGH. The device automatically initiates a new conversion and the cycle repeats.

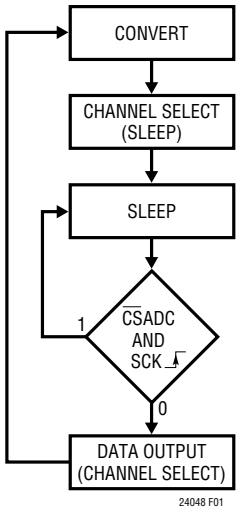


Figure 1. LTC2408 State Transition Diagram

Through timing control of the $\overline{CS}$ADC and SCK pins, the LTC2404/LTC2408 offer two modes of operation: internal or external SCK. These modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Conversion Clock

A major advantage delta-sigma converters offer over conventional type converters is an on-chip digital filter (commonly known as Sinc or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50 or 60Hz plus their harmonics. In order to reject these frequencies in excess of 110dB, a highly accurate conversion clock is required. The LTC2404/LTC2408 incorporate an on-chip highly accurate oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators. Clocked by the on-chip oscillator, the LTC2404/LTC2408 reject line frequencies (50 or 60Hz ±2%) a minimum of 110dB.

APPLICATIONS INFORMATION

Ease of Use

The LTC2404/LTC2408 data output has no latency, filter settling or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing an analog input voltage is easy.

The LTC2404/LTC2408 perform offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2404/LTC2408 automatically enter an internal reset state when the power supply voltage V_{CC} drops below approximately 2.2V. When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with duration of approximately 0.5ms. The POR signal clears all internal registers within the ADC and initiates a conversion. At power-up, the multiplexer channel is disabled and should be programmed once the device enters the sleep state. The results of the first conversion following a POR are not valid since a multiplexer channel was disabled.

Reference Voltage Range

The LTC2404/LTC2408 can accept a reference voltage from 0V to V_{CC}. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in microvolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a reduced reference voltage will improve the overall converter INL performance. The recommended range for the LTC2404/LTC2408 voltage reference is 100mV to V_{CC}.

Input Voltage Range

The converter is able to accommodate system level offset and gain errors as well as system level overrange situations due to its extended input range, see Figure 2.

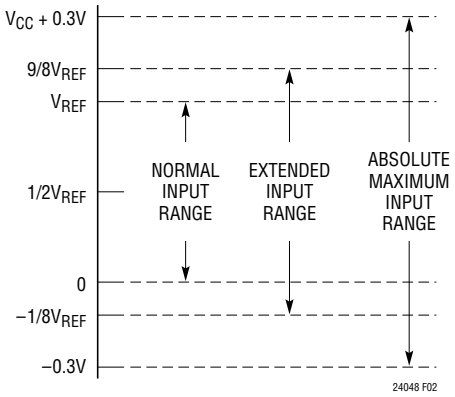


Figure 2. LTC2404/LTC2408 Input Range

The LTC2404/LTC2408 converts input signals within the extended input range of $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$.

For large values of V_{REF} this range is limited to a voltage range of –0.3V to (V_{CC} + 0.3V). Beyond this range the input ESD protection devices begin to turn on and the errors due to the input leakage current increase rapidly.

Input signals applied to V_{IN} may extend below ground by –300mV and above V_{CC} by 300mV. In order to limit any fault current, a resistor of up to 5k may be added in series with any channel input pin (CH0 to CH7) without affecting the performance of the device. In the physical layout, it is important to maintain the parasitic capacitance of the connection between this series resistance and the channel input pin as low as possible; therefore, the resistor should be located as close as practical to the channel input pin. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Analog Input/Reference Current section. In addition, a series resistor will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

Output Data Format

The LTC2404/LTC2408 serial output data stream is 32 bits long. The first 4 bits represent status information indicating the sign, input range and conversion state. The next 24 bits are the conversion result, MSB first. The remaining 4 bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution.

APPLICATIONS INFORMATION

Bit 31 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ADC pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is HIGH. If V_{IN} is <0, this bit is LOW. The sign bit changes state during the zero code.

Bit 28 (forth output bit) is the extended input range (EXR) indicator. If the input is within the normal input range $0 \le V_{IN} \le V_{REF}$, this bit is LOW. If the input is outside the normal input range, $V_{IN} > V_{REF}$ or $V_{IN} < 0$, this bit is HIGH.

The function of these bits is summarized in Table 1.

Table 1. LTC2404/LTC2408 Status Bits

Input Range	Bit 31 $\overline{EOC}$	Bit 30 DMY	Bit 29 SIG	Bit 28 EXR
$V_{IN} > V_{REF}$	0	0	1	1
$0 < V_{IN} \le V_{REF}$	0	0	1	0
$V_{IN} = 0^+/0^-$	0	0	1/0	0
$V_{IN} < 0$	0	0	0	1

Bit 27 (fifth output bit) is the most significant bit (MSB).

Bits 27-4 are the 24-bit conversion result MSB first.

Bit 4 is the least significant bit (LSB).

Bits 3-0 are sub LSBs below the 24-bit level. Bits 3-0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever $\overline{CS}$ADC is HIGH, SDO remains high impedance and any SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, $\overline{CS}$ADC must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ADC is pulled LOW. $\overline{EOC}$ changes in real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating a new conversion cycle has been initiated. This bit serves as $\overline{EOC}$ (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the V_{IN} pin is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any input value from $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$. For input voltages greater than $1.125 \cdot V_{REF}$, the conversion result is clamped to the value corresponding to $1.125 \cdot V_{REF}$. For input voltages below $-0.125 \cdot V_{REF}$, the conversion result is clamped to the value corresponding to $-0.125 \cdot V_{REF}$.

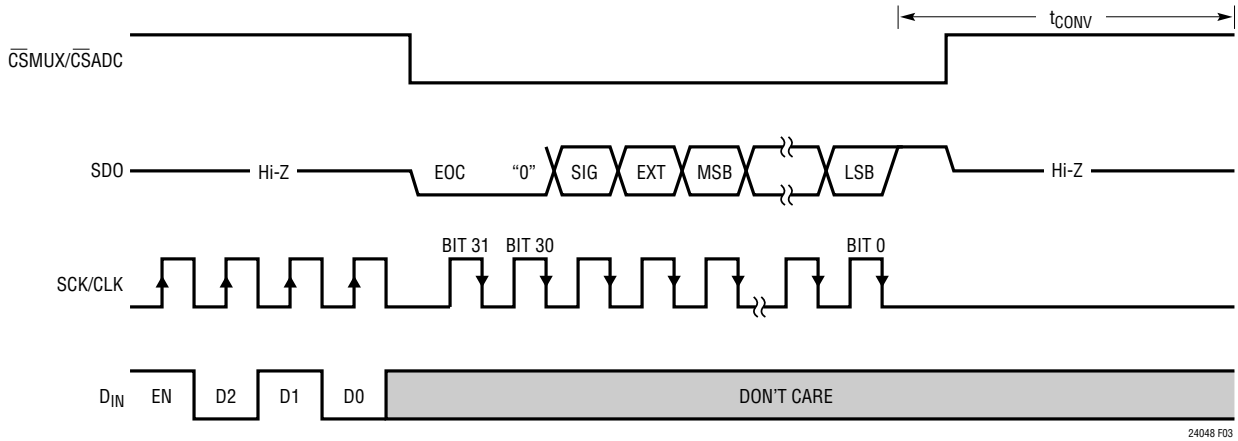


Figure 3. Typical Data Input/Output Timing

APPLICATIONS INFORMATION

Channel Selection

Typically, $\overline{CS}$ADC and $\overline{CS}$MUX are tied together or $\overline{CS}$ADC is inverted and drives $\overline{CS}$MUX. SCK and CLK are tied together and driven with a common clock signal. During channel selection, $\overline{CS}$MUX is HIGH. Data is shifted into the D_{IN} pin on the rising edge of CLK, see Figure 3. Table 3 shows the bit combinations for channel selection. In order to enable the multiplexer output, $\overline{CS}$MUX must be pulled LOW. The multiplexer should be programmed after the previous conversion is complete. In order to guarantee the conversion is complete, the multiplexer addressing should be delayed a minimum t_{CONV} (approximately 133ms for a 60Hz notch) after the data out is read.

While the multiplexer is being programmed, the ADC is in a low power sleep state. Once the MUX addressing is complete, the data from the preceding conversion can be read. A new conversion cycle is initiated following the data read cycle with the analog input tied to the newly selected channel.

Table 3. Logic Table for Channel Selection

CHANNEL STATUS	EN	D2	D1	D0
All Off	0	X	X	X
CH0	1	0	0	0
CH1	1	0	0	1
CH2	1	0	1	0
CH3	1	0	1	1
CH4*	1	1	0	0
CH5*	1	1	0	1
CH6*	1	1	1	0
CH7*	1	1	1	1

*Not used for the LTC2404.

Frequency Rejection Selection (F_O Pin Connection)

The LTC2404/LTC2408 internal oscillator provides better than 110dB normal mode rejection at the line frequency and all its harmonics for 50Hz ±2% or 60Hz ±2%. For 60Hz rejection, F_O (Pin 26) should be connected to GND (Pin 1) while for 50Hz rejection the F_O pin should be connected to V_{CC} (Pin 2).

Table 2. LTC2404/LTC2408 Output Data Format

Input Voltage	Bit 31 $\overline{EOC}$	Bit 30 DMY	Bit 29 SIG	Bit 28 EXR	Bit 27 MSB	Bit 26	Bit 25	Bit 24	Bit 23	…	Bit 4 LSB	Bit 3-0 SUB LSBs*
$V_{IN} > 9/8 \cdot V_{REF}$	0	0	1	1	0	0	0	1	1	...	1	X
$9/8 \cdot V_{REF}$	0	0	1	1	0	0	0	1	1	...	1	X
V_{REF} + 1LSB	0	0	1	1	0	0	0	0	0	...	0	X
V_{REF}	0	0	1	0	1	1	1	1	1	...	1	X
$3/4V_{REF}$ + 1LSB	0	0	1	0	1	1	0	0	0	...	0	X
$3/4V_{REF}$	0	0	1	0	1	0	1	1	1	...	1	X
$1/2V_{REF}$ + 1LSB	0	0	1	0	1	0	0	0	0	...	0	X
$1/2V_{REF}$	0	0	1	0	0	1	1	1	1	...	1	X
$1/4V_{REF}$ + 1LSB	0	0	1	0	0	1	0	0	0	...	0	X
$1/4V_{REF}$	0	0	1	0	0	0	1	1	1	...	1	X
$0^+/0^-$	0	0	1/0**	0	0	0	0	0	0	...	0	X
–1LSB	0	0	0	1	1	1	1	1	1	...	1	X
$-1/8 \cdot V_{REF}$	0	0	0	1	1	1	1	0	0	...	0	X
$V_{IN} < -1/8 \cdot V_{REF}$	0	0	0	1	1	1	1	0	0	...	0	X

*The sub LSBs are valid conversion results beyond the 24-bit level that may be included in averaging or discarded without loss of resolution.
**The sign bit changes state during the 0 code.

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The selection of 50Hz or 60Hz rejection can also be made by driving F_O to an appropriate logic level. A selection change during the sleep or data output states will not disturb the converter operation. If the selection is made during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected.

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be synchronized with an outside source, the LTC2404/LTC2408 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the F_O pin and turns off the internal oscillator. The frequency f_{EOSC} of the external signal must be at least 2560Hz (1Hz notch frequency) to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods t_{HEO} and t_{LEO} are observed.

While operating with an external conversion clock of a frequency f_{EOSC}, the LTC2404/LTC2408 provide better than 110dB normal mode rejection in a frequency range $f_{EOSC}/2560 \pm 4\%$ and its harmonics. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/2560$ is shown in Figure 4.

Whenever an external clock is not present at the F_O pin the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The

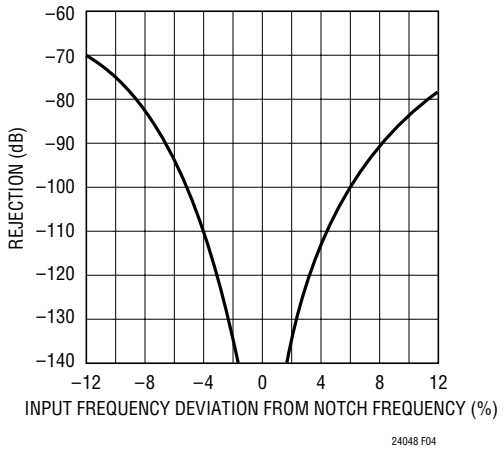

Figure 4. LTC2404/LTC2408 Normal Mode Rejection When Using an External Oscillator of Frequency f_{EOSC}

LTC2404/LTC2408 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

Table 4 summarizes the duration of each state as a function of F_O.

Table 4. LTC2404/LTC2408 State Duration

State	Operating Mode		Duration
CONVERT	Internal Oscillator	F_O = LOW (60Hz Rejection)	133ms
		F_O = HIGH (50Hz Rejection)	160ms
	External Oscillator	F_O = External Oscillator with Frequency f_{EOSC} kHz ($f_{EOSC}/2560$ Rejection)	$20480/f_{EOSC}$ (In Seconds)
SLEEP			As Long As $\overline{CS}$ = HIGH Until $\overline{CS}$ = 0 and SCK ↓
DATA OUTPUT	Internal Serial Clock	F_O = LOW/HIGH (Internal Oscillator)	As Long As $\overline{CS}$ = LOW But Not Longer Than 1.67ms (32 SCK cycles)
		F_O = External Oscillator with Frequency f_{EOSC} kHz	As Long As $\overline{CS}$ = LOW But Not Longer Than $256/f_{EOSC}$ms (32 SCK cycles)
	External Serial Clock with Frequency f_{SCK} kHz		As Long As $\overline{CS}$ = LOW But Not Longer Than $32/f_{SCK}$ms (32 SCK cycles)
MAXIMUM OUTPUT WORD RATE			$OWR = \frac{1}{t_{CONVERT} + t_{DATAOUTPUT}}$ in Hz

APPLICATIONS INFORMATION

Using an External Clock for Faster Conversion Times

The conversion time of the LTC2404/LTC2408 is determined by the conditions on the F_O pin. If F_O is connected to GND for 60Hz rejection, the conversion time is 133µs. If F_O is connected to V_{CC}, the conversion time is 160µs. For an externally supplied frequency of f_{EOSC}(kHz), the conversion time is:

$t_{CONV} = 20480/f_{EOSC}$ (kHz)

The resulting frequency rejection is:

Notch Frequency = $8/t_{CONV}$

The maximum output word rate is:

$$OWR = \frac{1}{t_{CONVERT} + t_{DATAOUTPUT}} \text{ in Hz}$$

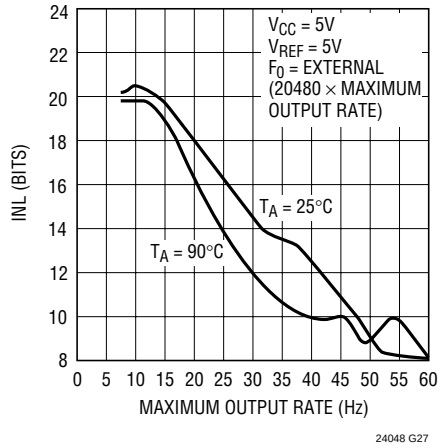

Figure 5. INL vs Maximum Output Rate

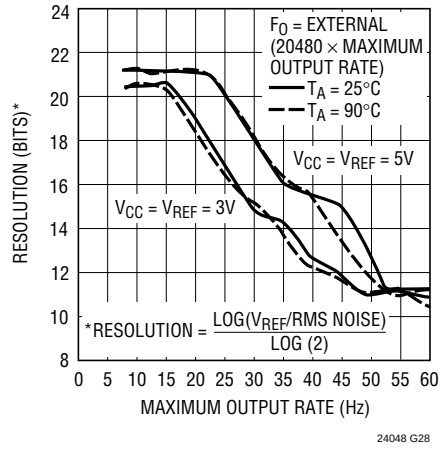

Figure 6. Resolution vs Maximum Output Rate

The DC specifications are guaranteed for f_{EOSC} up to a maximum of 307.2kHz, resulting in a maximum output word rate of approximately 15Hz. However, for faster rates at reduced performance, frequencies up to 1.22MHz can be used on the F_O pin. Figures 5 and 6 show the INL and Resolution vs Output Rate.

SERIAL INTERFACE

The LTC2404/LTC2408 transmit the conversion results, program the channel selection, and receive the start of conversion command through a synchronous 4-wire interface (SCK = CLK, $\overline{CS}$ADC = $\overline{CS}$MUX). During the conversion and sleep states, this interface can be used to assess the converter status. While in the sleep state this interface may be used to program an input channel. During the data output state it is used to read the conversion result.

ADC Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 25) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2404/LTC2408 creates its own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected on power-up and then reselected every time a HIGH-to-LOW transition is detected at the $\overline{CS}$ADC pin. If SCK is HIGH or floating at power-up or during this transition, the converter enters the internal SCK mode. If SCK is LOW at power-up or during this transition, the converter enters the external SCK mode.

Multiplexer Serial Input Clock (CLK)

Generally, this pin is externally tied to SCK for 4-wire operation. On the rising edge of CLK (Pin 19) with $\overline{CS}$MUX held HIGH, data is serially shifted into the multiplexer. If $\overline{CS}$MUX is LOW the CLK input will be disabled and the channel selection unchanged.

Serial Data Output (SDO)

The serial data output pin, SDO (Pin 24), drives the serial data during the data output state. In addition, the SDO pin

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is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{CS}$ADC (Pin 23) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If $\overline{CS}$ADC is LOW during the convert or sleep state, SDO will output $\overline{EOC}$. If $\overline{CS}$ADC is LOW during the conversion phase, the $\overline{EOC}$ bit appears HIGH on the SDO pin. Once the conversion is complete, $\overline{EOC}$ goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while $\overline{CS}$ADC = 0.

ADC Chip Select Input ($\overline{CS}$ADC)

The active LOW chip select, $\overline{CS}$ADC (Pin 23), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the $\overline{CS}$ADC signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2404/LTC2408 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the $\overline{CS}$ADC pin after the converter has entered the data output state (i.e., after the first rising edge of SCK occurs with $\overline{CS}$ADC = 0).

Multiplexer Chip Select ($\overline{CS}$MUX)

For 4-wire operation, this pin is tied directly to $\overline{CS}$ADC or the output of an inverter tied to $\overline{CS}$ADC. $\overline{CS}$MUX (Pin 20) is driven HIGH during selection of a multiplexer channel. On the falling edge of $\overline{CS}$MUX, the selected channel is enabled and drives MUXOUT.

Data Input (D_{IN})

The data input to the multiplexer, D_{IN} (Pin 21), is used to program the multiplexer. The input channel is selected by serially shifting a 4-bit input word into the D_{IN} pin under the control of the multiplexer clock, CLK. Data is shifted into the multiplexer on the rising edge of CLK. Table 3 shows the logic table for channel selection. In order to select or change a previously programmed channel, an enable bit (D_{IN} = 1) must proceed the 3-bit channel select serial data. The user may set D_{IN} = 0 to continually convert on the previously selected channel.

SERIAL INTERFACE TIMING MODES

The LTC2404/LTC2408's 4-wire interface is SPI and MICROWIRE compatible. This interface offers two modes of operation. These include an internal or external serial clock. The following sections describe both of these serial interface timing modes in detail. For both cases the converter can use the internal oscillator (F_O = LOW or F_O = HIGH) or an external oscillator connected to the F_O pin. Refer to Table 5 for a summary.

External Serial Clock (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock (SCK) to shift out the conversion result, see Figure 7. This same external clock signal drives the CLK pin in order to program the multiplexer. A single $\overline{CS}$ signal drives both the multiplexer $\overline{CS}$MUX and converter $\overline{CS}$ADC inputs. This common signal is used to monitor and control the state of the conversion as well as enable the channel selection.

The serial clock mode is selected on the falling edge of $\overline{CS}$ADC. To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each $\overline{CS}$ADC falling edge.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ADC is HIGH. At any time during the conversion cycle, $\overline{CS}$ADC may be pulled LOW in order to monitor the state of the converter. While $\overline{CS}$ADC is LOW, $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state. Independent of $\overline{CS}$ADC, the device automatically enters the low power sleep state once the conversion is complete.

Table 5. LTC2404/LTC2408 Interface Timing Modes

Configuration	SCK Source	Conversion Cycle Control	Data Output Control	Connection and Waveforms
External SCK	External	$\overline{CS}$ and SCK	$\overline{CS}$ and SCK	Figures 7, 8, 9
Internal SCK	Internal	$\overline{CS}$ ↓	CS ↓	Figures 10, 11

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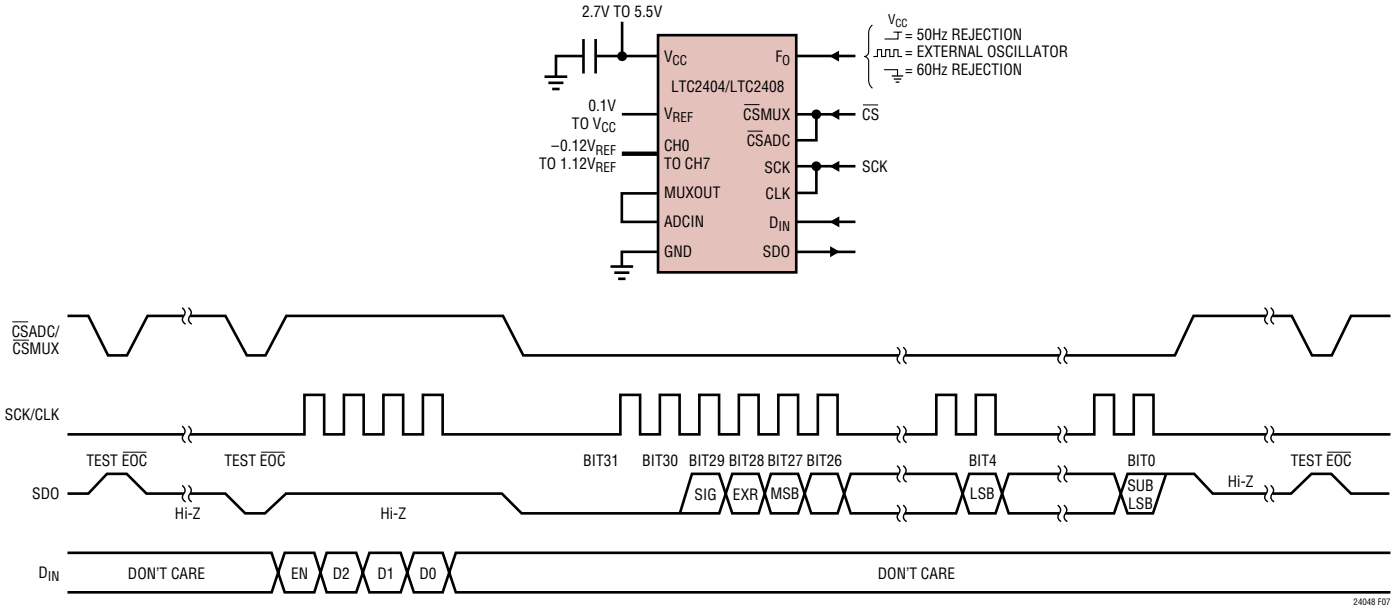

Figure 7. External Serial Clock Timing Diagram

While the device is in the sleep state, prior to entering the data output state, the user may program the multiplexer. As shown in Figure 7, the multiplexer channel is selected by serial shifting a 4-bit word into the D_{IN} pin on the rising edge of CLK (CLK is tied to SCK). The first bit is an enable bit that must be HIGH in order to program a channel. The next three bits determine which channel is selected, see Table 3. On the falling edge of $\overline{CS}$MUX, the new channel is selected and will be valid for the first conversion performed following the data output state. Clock signals applied to the CLK pin while $\overline{CS}$MUX is LOW (during the data output state) will have no effect on the channel selection. Furthermore, if D_{IN} is held LOW or CLK is held LOW during the sleep state, the channel selection is unchanged.

When the device is in the sleep state ($\overline{EOC}$ = 0), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while $\overline{CS}$ADC is LOW. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC}$ = 1) indicating a conversion is in progress.

At the conclusion of the data cycle, $\overline{CS}$ADC may remain LOW and $\overline{EOC}$ monitored as an end-of-conversion interrupt. Alternatively, $\overline{CS}$ADC may be driven HIGH setting SDO to Hi-Z. As described above, $\overline{CS}$ADC may be pulled LOW at any time in order to monitor the conversion status. For each of these operations, $\overline{CS}$MUX may be tied to $\overline{CS}$ADC without affecting the selected channel.

At the conclusion of the data output cycle, the converter enters a user transparent calibration cycle prior to actually performing a conversion on the selected input channel. This enables a 66ms (for 60Hz notch frequency) look ahead time for the multiplexer input. Following the data output cycle, the multiplexer input channel may be selected any time in this 66ms window by pulling $\overline{CS}$ADC HIGH and serial shifting data into the D_{IN} pin, see Figure 8.

While the device is performing the internal calibration, it is sensitive to ground current disturbances. Error currents flowing in the ground pin may lead to offset errors. If the SCK pin is toggling during the calibration, these ground disturbances will occur. The solution is to either drive the multiplexer clock input (CLK) separately from the ADC clock input (SCK), or program the multiplexer in the first 1ms following the data output cycle. The remaining 65ms may be used to allow the input signal to settle.

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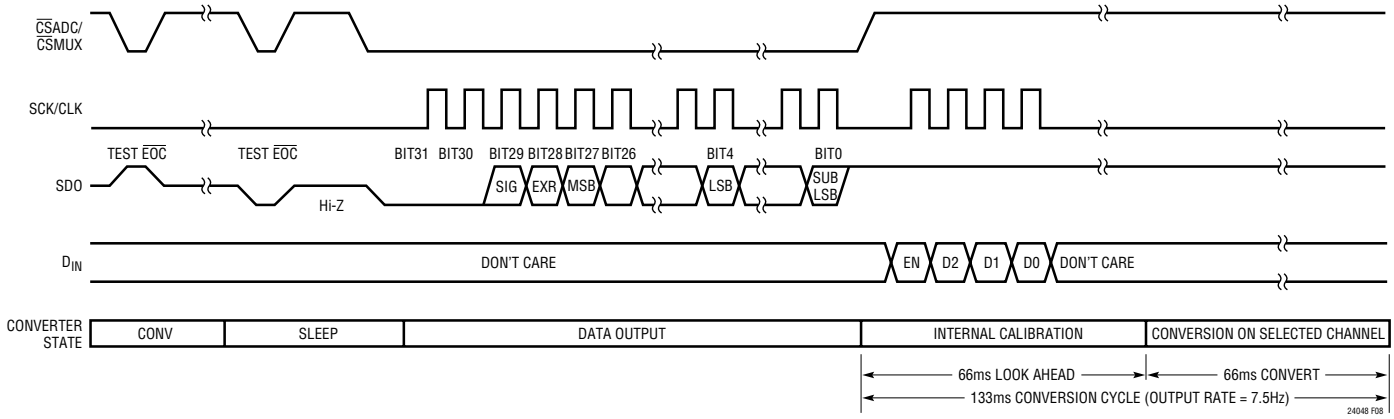

Figure 8. Use of Look Ahead to Program Multiplexer After Data Output

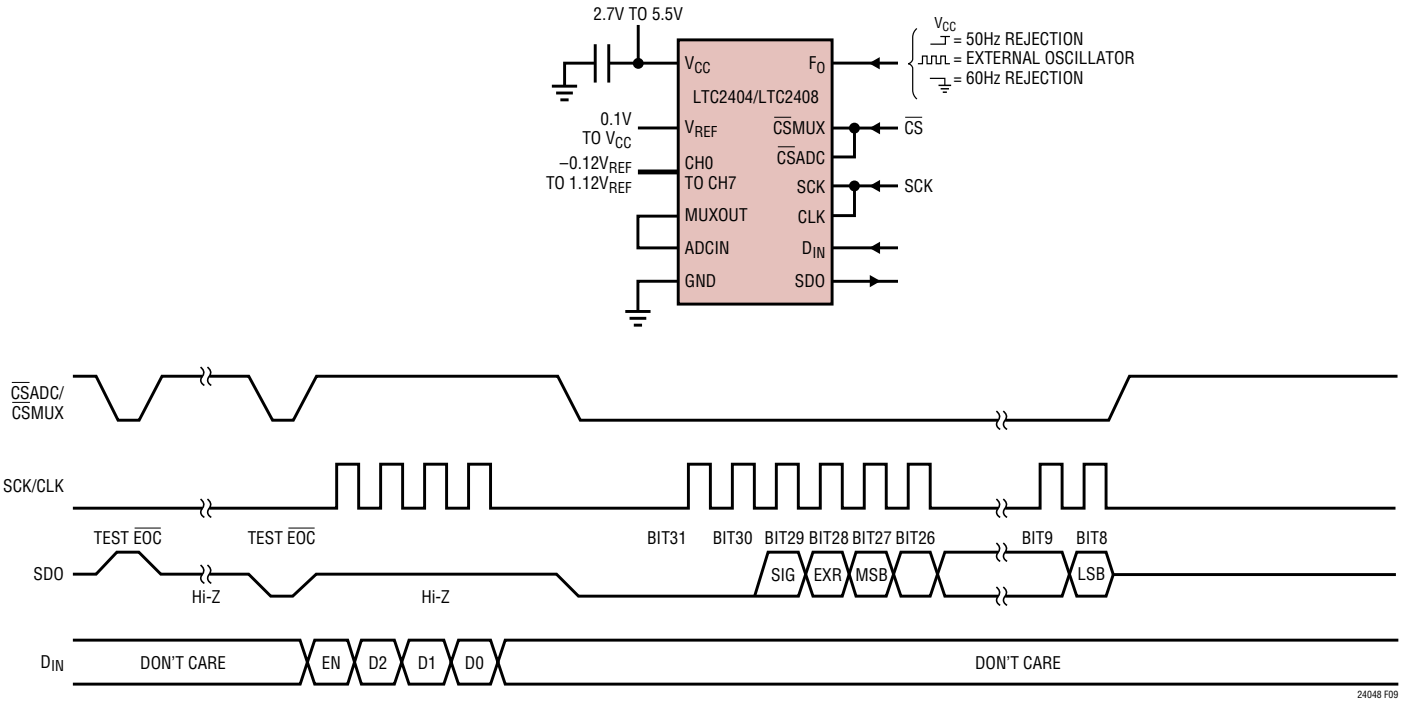

Figure 9. External Serial Clock with Reduced Data Output Length Timing Diagram

Typically, $\overline{CS}$ADC remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ADC HIGH anytime between the first rising edge and the 32nd falling edge of SCK, see Figure 9. On the rising edge of $\overline{CS}$ADC, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

Internal Serial Clock

This timing mode uses an internal serial clock to shift out the conversion result and program the multiplexer, see Figure 10. A $\overline{CS}$ signal directly drives the $\overline{CS}$ADC input, while the inverse of $\overline{CS}$ drives the $\overline{CS}$MUX input. The $\overline{CS}$ signal is used to monitor and control the state of the conversion cycles as well as enable the channel selection. The multiplexer is programmed during the data output

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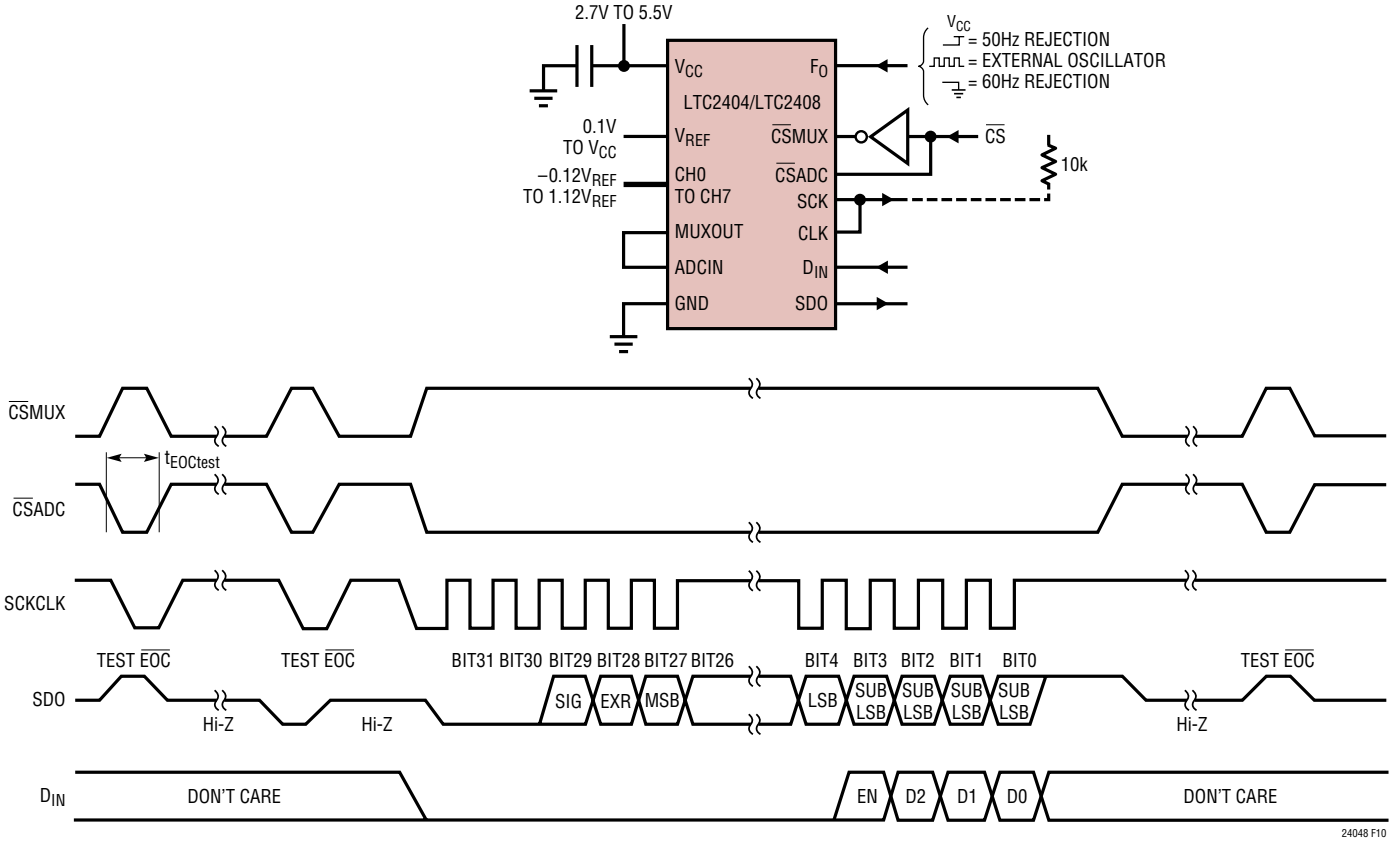

Figure 10. Internal Serial Clock Timing Diagram

state. The internal serial clock (SCK) generated by the ADC is applied to the multiplexer clock input (CLK).

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (Hi-Z) or pulled HIGH prior to the falling edge of $\overline{CS}$ADC. The device will not enter the internal serial clock mode if SCK is driven LOW on the falling edge of $\overline{CS}$ADC. An internal weak pull-up resistor is active on the SCK pin during the falling edge of $\overline{CS}$ADC; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ADC is HIGH. At any time during the conversion cycle, $\overline{CS}$ADC may be pulled LOW in order to monitor the state of the converter. Once $\overline{CS}$ADC is pulled LOW, SCK goes LOW and $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state.

When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit the sleep state and enter the data output state if $\overline{CS}$ADC remains LOW. In order to prevent the device from exiting the low power sleep state, $\overline{CS}$ADC must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of $\overline{CS}$ADC (if $\overline{EOC}$ = 0) or $t_{EOCtest}$ after $\overline{EOC}$ goes LOW (if $\overline{CS}$ADC is LOW during the falling edge of $\overline{EOC}$). The value of $t_{EOCtest}$ is 23µs if the device is using its internal oscillator (F_O = logic LOW or HIGH). If F_O is driven by an external oscillator of frequency f_{EOSC}, then $t_{EOCtest}$ is $3.6/f_{EOSC}$. If $\overline{CS}$ADC is pulled HIGH before time $t_{EOCtest}$, the device remains in the sleep state. The conversion result is held in the internal static shift register.

If $\overline{CS}$ADC remains LOW longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle begins on this first rising edge of SCK and concludes after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output

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to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC}$ = 1), SCK stays HIGH, and a new conversion starts.

While operating in the internal serial clock mode, the SCK output of the ADC may be used as the multiplexer clock (CLK). D_{IN} is latched into the multiplexer on the rising edge of CLK. As shown in Figure 10, the multiplexer channel is selected by serial shifting a 4-bit word into the D_{IN} pin on the rising edge of CLK. The first bit is an enable bit which must be HIGH in order to program a channel. The next three bits determine which channel is selected, see Table 3. On the rising edge of $\overline{CS}$ADC (falling edge of $\overline{CS}$MUX), the new channel is selected and will be valid for the next conversion. If D_{IN} is held LOW during the data output state, the previous channel selection remains valid.

Typically, $\overline{CS}$ADC remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ADC HIGH anytime between the first and 32nd rising edge of SCK, see Figure 11. On the rising edge of $\overline{CS}$ADC, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. If $\overline{CS}$ADC is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of $\overline{CS}$ADC. This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling $\overline{CS}$ADC HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2404/LTC2408's internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing

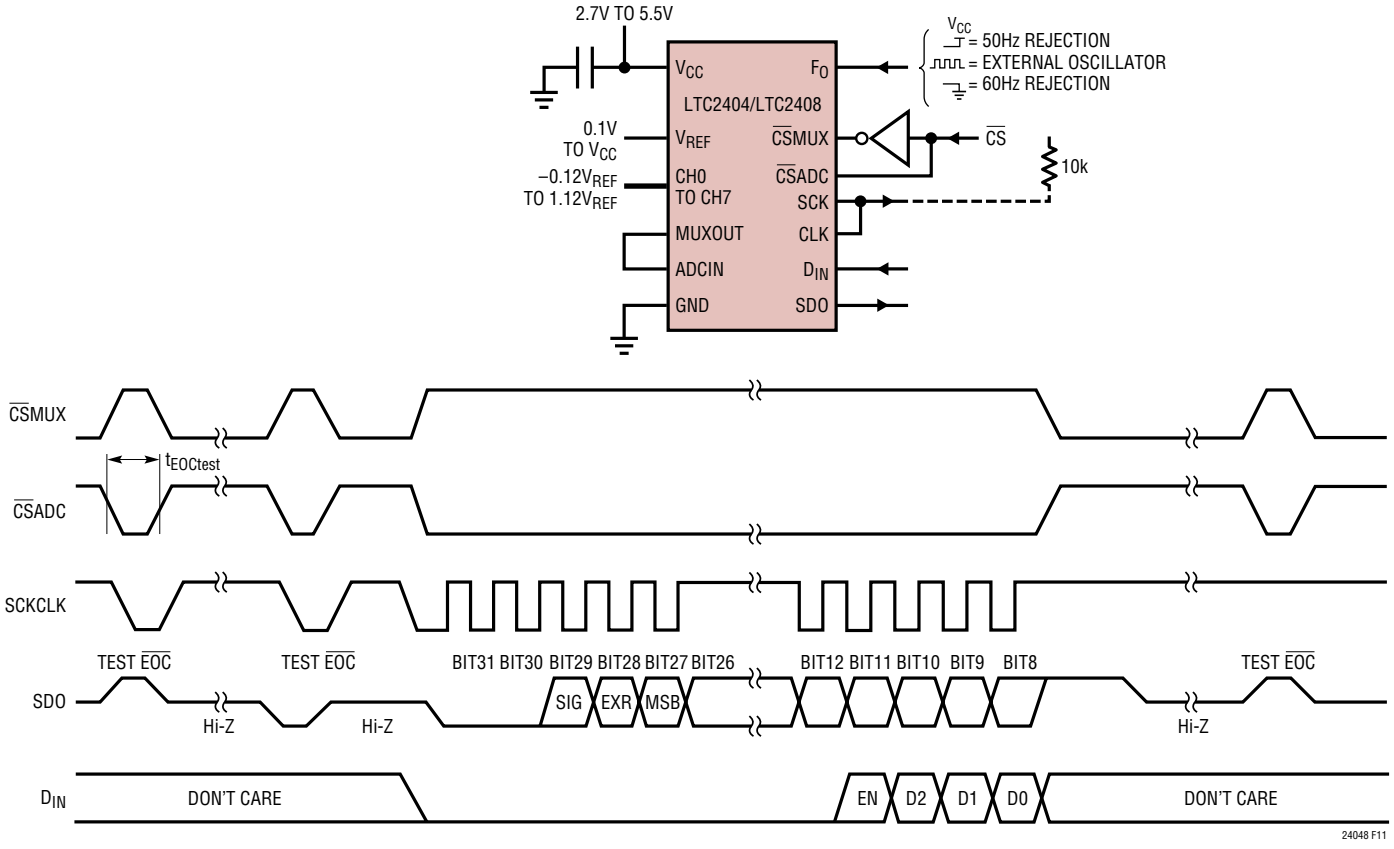

Figure 11. Internal Serial Clock with Reduced Data Output Length Timing Diagram

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mode. However, certain applications may require an external driver on SCK. If this driver goes Hi-Z after outputting a LOW signal, the LTC2404/LTC2408's internal pull-up remains disabled. Hence, SCK remains LOW. On the next falling edge of $\overline{CS}$ADC, the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes Hi-Z. On the next $\overline{CS}$ADC falling edge, the device will remain in the internal SCK timing mode.

A similar situation may occur during the sleep state when $\overline{CS}$ADC is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state ($\overline{EOC}$ = 0), SCK will go LOW. Once $\overline{CS}$ADC goes HIGH (within the time period defined above as $t_{EOCtest}$), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK to a HIGH level before $\overline{CS}$ADC goes LOW again. This is not a concern under normal conditions where $\overline{CS}$ADC remains LOW after detecting $\overline{EOC}$ = 0. This situation is easily avoided by adding an external 10k pull-up resistor to the SCK pin.

DIGITAL SIGNAL LEVELS

The LTC2404/LTC2408's digital interface is easy to use. Its digital inputs (F_O, $\overline{CS}$ADC, $\overline{CS}$MUX, CLK, D_{IN} and SCK in External SCK mode of operation) accept standard TTL/CMOS logic levels and can tolerate edge rates as slow as 100µs. However, some considerations are required to take advantage of exceptional accuracy and low supply current.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

In order to preserve the accuracy of the LTC2404/LTC2408, it is very important to minimize the ground path impedance which may appear in series with the input and/or reference signal and to reduce the current which may flow through this path. Pin 6 (GND) should be connected to a low resistance ground plane through a minimum length trace. The use of multiple via holes is recommended to further reduce the connection resistance. The LTC2404/LTC2408's power supply current flowing through the 0.01Ω resistance of the common ground pin will develop a 2.5µV offset signal. For a reference voltage V_{REF} = 2.5V, this represents a 1ppm offset error.

In an alternative configuration, Pin 6 (GND) of the converter can be the single-point-ground in a single point grounding system. The input signal ground, the reference signal ground, the digital drivers ground (usually the digital ground) and the power supply ground (the analog ground) should be connected in a star configuration with the common point located as close to Pin 6 as possible.

The power supply current during the conversion state should be kept to a minimum. This is achieved by restricting the number of digital signal transitions occurring during this period.

While a digital input signal is in the 0.5V to (V_{CC} – 0.5V) range, the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals (F_O, $\overline{CS}$ADC, $\overline{CS}$MUX, D_{IN}, CLK and SCK in External SCK mode of operation) is within this range, the LTC2404/LTC2408 power supply current may increase even if the signal in question is at a valid logic level. For micropower operation and in order to minimize the potential errors due to additional ground pin current, it is recommended to drive all digital input signals to full CMOS levels [V_{IL} < 0.4V and V_{OH} > (V_{CC} – 0.4V)].

Severe ground pin current disturbances can also occur due to the undershoot of fast digital input signals. Undershoot and overshoot can occur because of the impedance mismatch at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to LTC2404/LTC2408. For reference, on a regular FR-4 board, signal propagation velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus, a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

Parallel termination near the LTC2404/LTC2408 input pins will eliminate this problem but will increase the driver

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power dissipation. A series resistor between 27Ω and 56Ω placed near the driver or near the LTC2404/LTC2408 pin will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

Driving the Input and Reference

The analog input and reference of the typical delta-sigma analog-to-digital converter are applied to a switched capacitor network. This network consists of capacitors switching between the analog input (ADCIN), ground and the reference (V_{REF}). The result is small current spikes seen at both ADCIN and V_{REF}. A simplified input equivalent circuit is shown in Figure 12.

The key to understanding the effects of this dynamic input current is based on a simple first order RC time constant model. Using the internal oscillator, the internal switched capacitor network of the LTC2404/LTC2408 is clocked at 153,600Hz corresponding to a 6.5μs sampling period. Fourteen time constants are required each time a capacitor is switched in order to achieve 1ppm settling accuracy.

Therefore, the equivalent time constant at V_{IN} and V_{REF} should be less than 6.5μs/14 = 460ns in order to achieve 1ppm accuracy.

Input Current (V_{IN})

If complete settling occurs on the input, conversion results will be uneffected by the dynamic input current. If the settling is incomplete, it does not degrade the linearity performance of the device. It simply results in an offset/full-scale shift, see Figure 13. To simplify the analysis of input dynamic current, two separate cases are assumed: large capacitance at V_{IN} (C_{IN} > 0.01μF) and small capacitance at V_{IN} (C_{IN} < 0.01μF).

If the total capacitance at V_{IN} (see Figure 14) is small (<0.01μF), relatively large external source resistances (up to 20k for 20pF parasitic capacitance) can be tolerated without any offset/full-scale error. Figures 15 and 16 show a family of offset and full-scale error curves for various

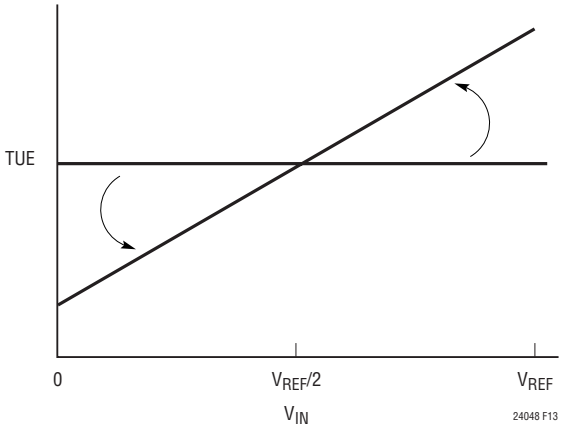

Figure 13. Offset/Full-Scale Shift

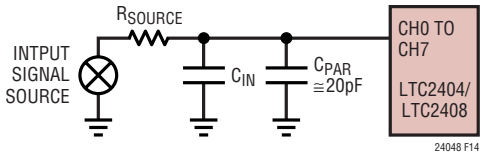

Figure 14. An RC Network at CH0 to CH7

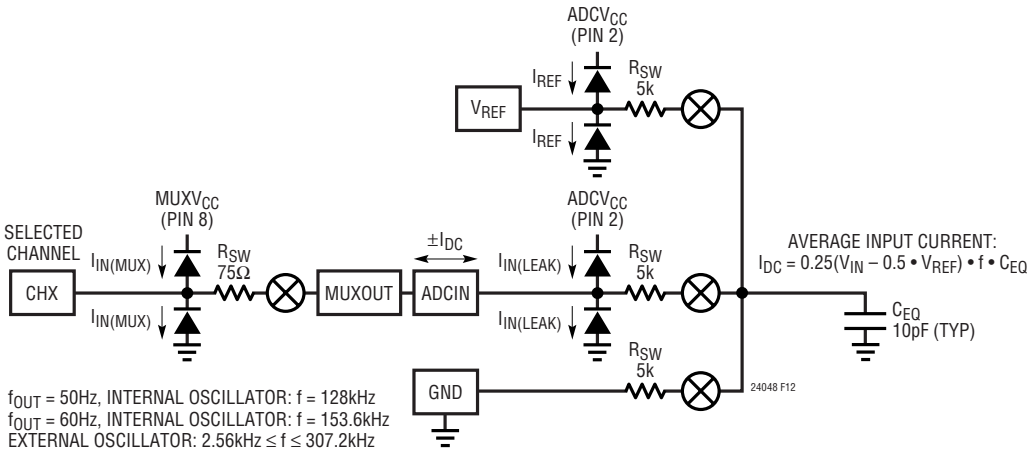

Figure 12. LTC2404/LTC2408 Equivalent Analog Input Circuit

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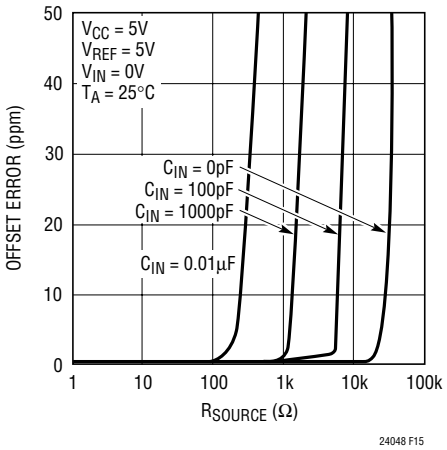

Figure 15. Offset vs R_{SOURCE} (Small C)

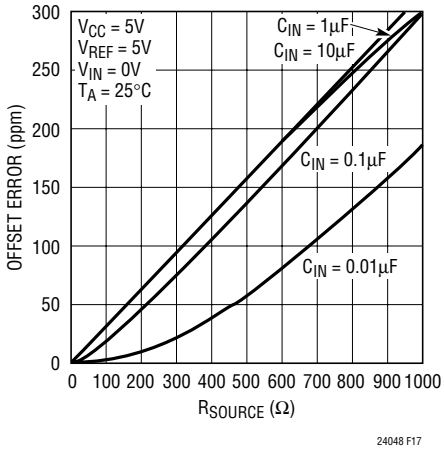

Figure 17. Offset vs R_{SOURCE} (Large C)

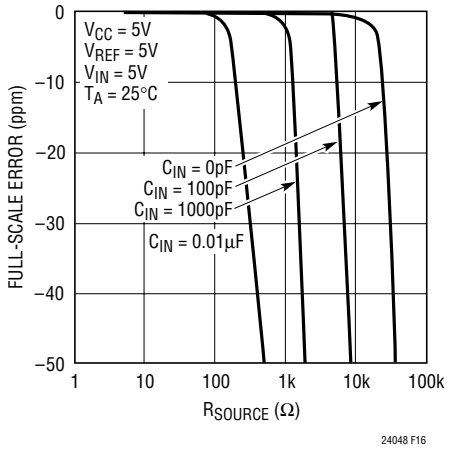

Figure 16. Full-Scale Error vs R_{SOURCE} (Small C)

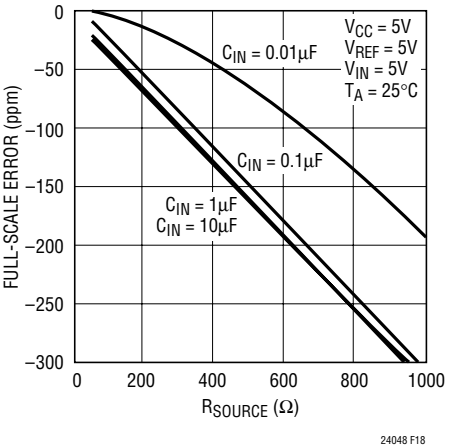

Figure 18. Full-Scale Error vs R_{SOURCE} (Large C)

small valued input capacitors (C_{IN} < 0.01µF) as a function of input source resistance.

For large input capacitor values (C_{IN} > 0.01µF), the input spikes are averaged by the capacitor into a DC current. The gain shift becomes a linear function of input source resistance independent of input capacitance, see Figures 17 and 18. The equivalent input impedance is 1.66MΩ. This results in ±1.5µA of input dynamic current at the extreme values of V_{IN} (V_{IN} = 0V and V_{IN} = V_{REF}, when V_{REF} = 5V). This corresponds to a 0.3ppm shift in offset and full-scale readings for every 1Ω of input source resistance.

While large capacitance applied to one of the multiplexer channel inputs may result in offset/full-scale shifts, large capacitance applied to the MUXOUT/ADCIN results in linearity errors. The 75Ω on-resistance of the multiplexer switch is nonlinear with input voltage. If the capacitance at node MUXOUT/ADCIN is less than 0.01µF, the linearity is not degraded. On the other hand, excessive capacitance (>0.01µF) results in incomplete settling as a function of the multiplexer on-resistance. Hence, the nonlinearity of the multiplexer switch is seen in the overall transfer characteristic.

In addition to the input current spikes, the input ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a fixed offset shift of 10µV for a 10k source resistance.

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Reference Current (V_{REF})

Similar to the analog input, the reference input has a dynamic input current. This current has negligible effect on the offset. However, the reference current at $V_{IN} = V_{REF}$ is similar to the input current at full-scale. For large values of reference capacitance ($C_{VREF} > 0.01\mu F$), the full-scale error shift is 0.3ppm/Ω of external reference resistance independent of the capacitance at V_{REF}, see Figure 19. If the capacitance tied to V_{REF} is small ($C_{VREF} < 0.01\mu F$), an input resistance of up to 20k (20pF parasitic capacitance at V_{REF}) may be tolerated, see Figure 20.

Unlike the analog input, the integral nonlinearity of the device can be degraded with excessive external RC time constants tied to the reference input. If the capacitance at node V_{REF} is small ($C_{VREF} < 0.01\mu F$), the reference input can tolerate large external resistances without reduction in INL, see Figure 21. If the external capacitance is large ($C_{VREF} > 0.01\mu F$), the linearity will be degraded by 0.15ppm/Ω independent of capacitance at V_{REF}, see Figure 22.

In addition to the dynamic reference current, the V_{REF} ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a fixed full-scale shift of 10μV for a 10k source resistance.

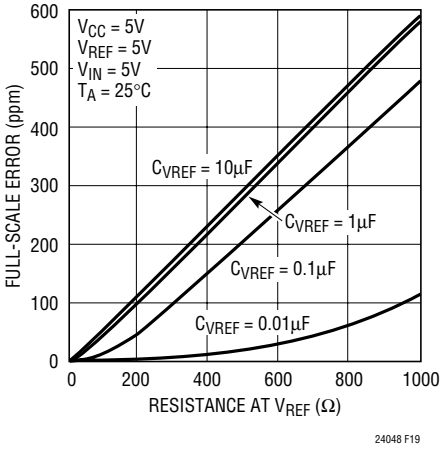

Figure 19. Full-Scale Error vs R_{VREF} (Large C)

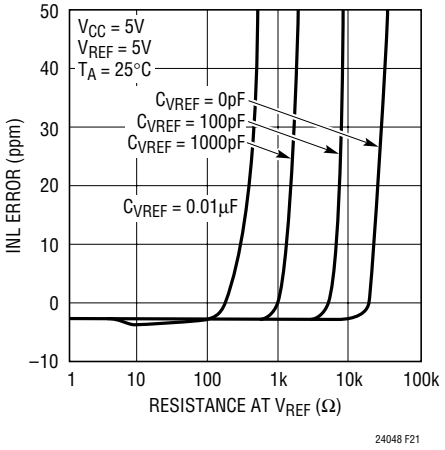

Figure 21. INL Error vs R_{VREF} (Small C)

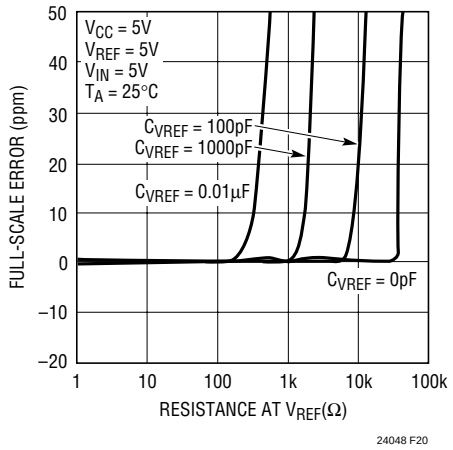

Figure 20. Full-Scale Error vs R_{VREF} (Small C)

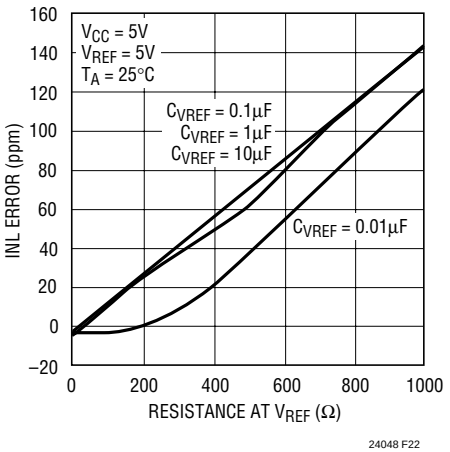

Figure 22. INL Error vs R_{VREF} (Large C)

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ANTIALIASING

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2404/LTC2408 significantly simplify antialiasing filter requirements.

The digital filter provides very high rejection except at integer multiples of the modulator sampling frequency (f_S), see Figure 23. The modulator sampling frequency is 256 • F_O, where F_O is the notch frequency (typically 50Hz or 60Hz). The bandwidth of signals not rejected by the digital filter is narrow (≈0.2%) compared to the bandwidth of the frequencies rejected.

As a result of the oversampling ratio (256) and the digital filter, minimal (if any) antialias filtering is required in front of the LTC2404/LTC2408. If passive RC components are placed in front of the LTC2404/LTC2408, the input dynamic current should be considered (see Input Current section). In cases where large effective RC time constants are used, an external buffer amplifier may be required to minimize the effects of input dynamic current.

The modulator contained within the LTC2404/LTC2408 can handle large-signal level perturbations without saturating. Signal levels up to 40% of V_{REF} do not saturate the analog modulator. These signals are limited by the input ESD protection to 300mV below ground and 300mV above V_{CC}.

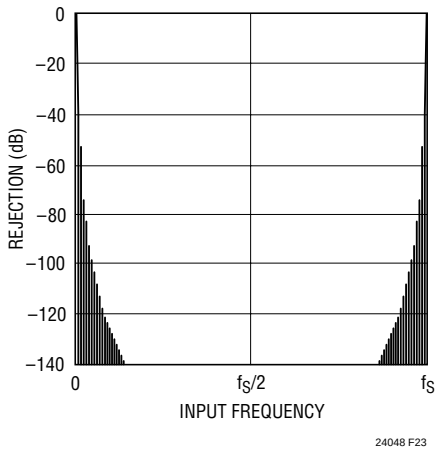

Figure 23. Sinc^4 Filter Rejection

The LTC2408's Resolution and Accuracy Allows You to Measure Points in a Ladder of Sensors

In many industrial processes, for example, cracking towers in petroleum refineries, a group of temperature measurements must be related to one another. A series of platinum RTDs that sense slow changing temperatures can be configured into a resistive ladder, using the LTC2408 to sense each node. This approach allows a single excitation current passed through the entire ladder, reducing total supply current consumption. In addition, this approach requires only one high precision resistor, thereby reducing cost. A group of up to seven temperatures can be measured as a group by a single LTC2408 in a loop-powered remote acquisition unit. In the example shown in Figure 24, the excitation current is 240μA at 0°C. The LTC2408 requires 300μA, leaving nearly 3.5mA for the remainder of the remote transmitter.

The resistance of any of the RTDs (PT1 to PT7) is determined from the voltage across it, as compared to the voltage drop across the reference resistor (R1). This is a ratiometric implementation where the voltage drop across R1 is given by $V_{REF} – V_{CH1}$. Channel 7 is used to measure the voltage on a representative length of wire. If the same type and length of wire is used for all connections, then errors associated with the voltage drops across all wiring can be removed in software. The contribution of wiring drop can be scaled if wire lengths are not equal.

Gain can be added to this circuit as the total voltage drop across all the RTDs is small compared to ADC full-scale range. The maximum recommended gain is 40, as limited by both amplifier noise contribution, as well as the maximum voltage developed at CH0 when all sensors are at the maximum temperature specified for platinum RTDs.

Adding gain requires that one of the resistors (PT1 to PT7) be a precision resistor in order to eliminate the error associated with the gain setting resistors R2 and R3. Note, that if a precision (100Ω to 400Ω) resistor is used in place of one of the RTDs (PT7 recommended), R1 does not need to be a high precision resistor. Although the substitution of a precision reference resistor for an RTD to determine gain may suggest that R2 and R3 (and R1) need not be precise, temperature fluctuations due to airflow may appear as noise that cannot be removed in firmware. Conse-

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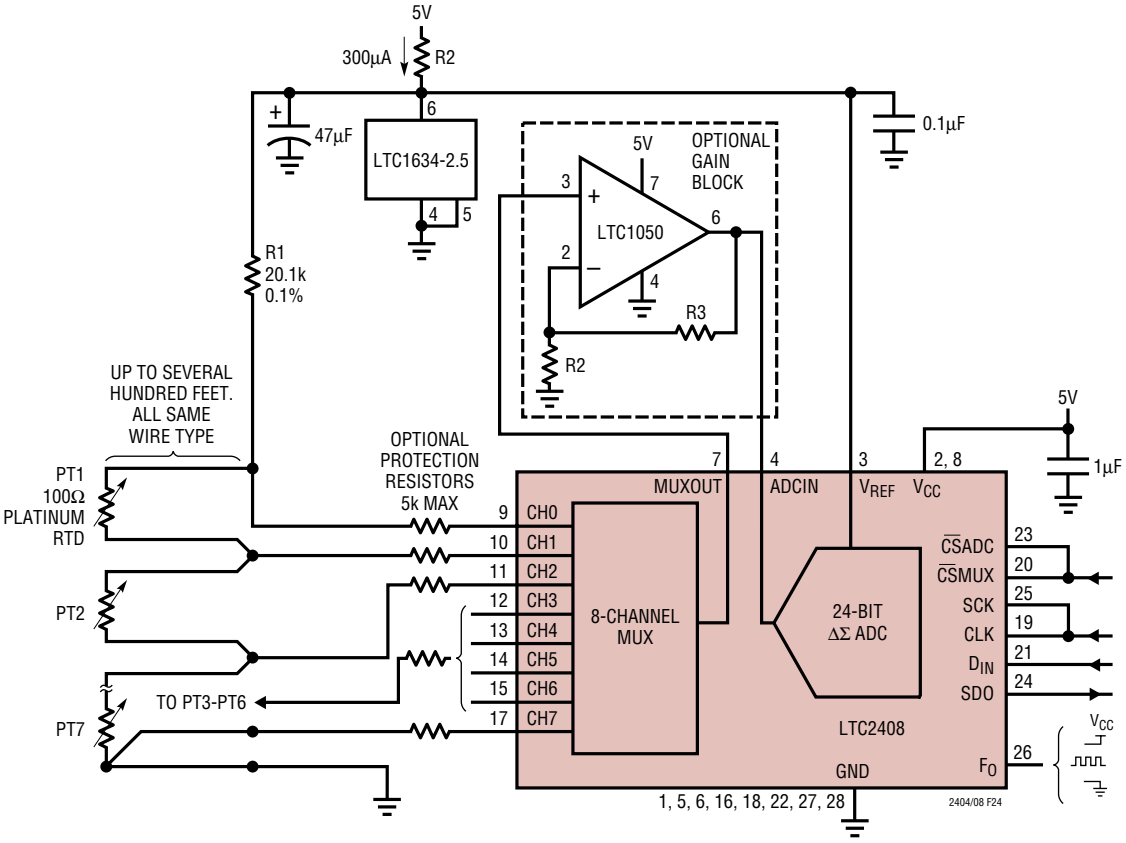

Figure 24. Measuring Up to Seven RTD Temperatures with One Reference Resistor and One Reference Current

quently, these resistors should be low temperature coefficient devices. The use of higher resistance RTDs is not recommended in this topology, although the inclusion of one 1000Ω RTD at the top on the ladder will have minimal impact on the lower elements. The same caveat applies to fast changing temperatures. Any fast changing sensors should be at the top of the ladder.

The LTC2408's Uncommitted Multiplexer Finds Use in a Programmable Gain Scheme

If the multiplexer in the LTC2408 is not committed to channel selection, it can be used to select various signal-processing options such as different gains, filters or attenuator characteristics. In Figure 25, the multiplexer is shown selecting different taps on an R/2R ladder in the feedback loop of an amplifier. This example allows selection of gain from 1 to 128 in binary steps. Other feedback networks could be used to provide gains tailored for specific purposes. (For example, 1x, 1.1x, 1.41x, 2x, 2.028x, 5x, 10x, 40x, etc.) Alternatively, different bandpass characteristics or signal inversion/noninversion could be selected. The R/2R ladder can be purchased as a network to ensure tight temperature tracking. Alternatively, resistors in a ladder or as separate dividers can be assembled from discrete resistors. In the configuration shown, the channel resistance of the multiplexer does not contribute much to the error budget, as only input op amp current flows through the switch. The LTC1050 was chosen for its low input current and offset voltage, as well as its ability to drive the input of a ΔΣ ADC.

Insert Gain or Buffering After the Multiplexer

Separate MUXOUT and ADCIN terminals permit insertion of a gain stage between the MUX and the ADC. If passive filtering is used at the input to the ADC, a buffer amplifier is strongly recommended to avoid errors resulting from the dynamic ADC input current. If antialiasing is required, it should be placed at the input to the MUX. If bandwidth limiting is required to improve noise performance, a filter with a –3dB point at 1500Hz will reduce the effective total

APPLICATIONS INFORMATION

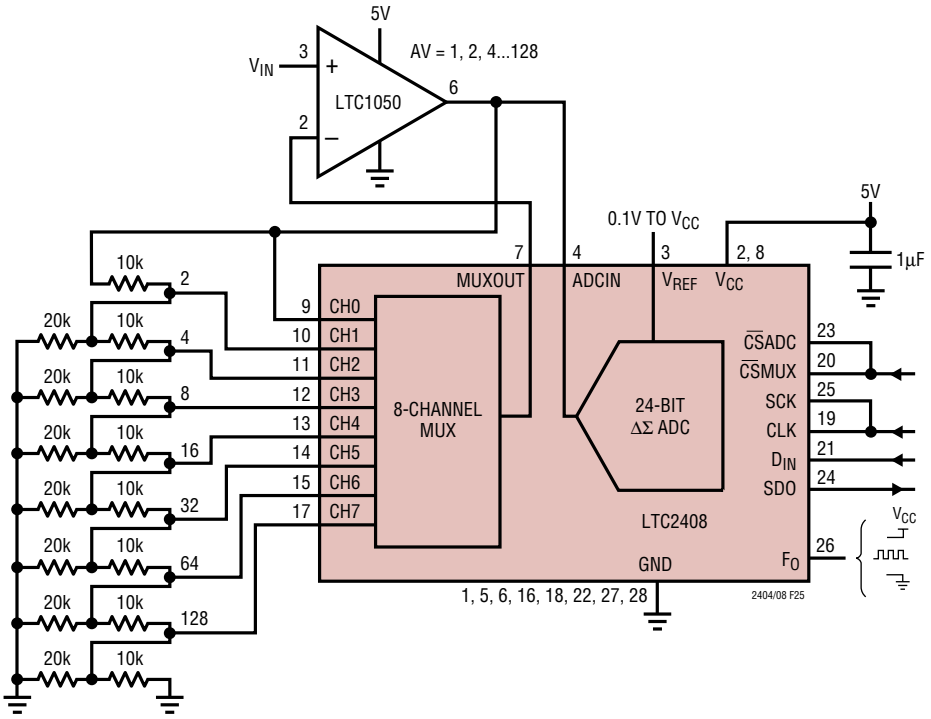

Figure 25. Using the Multiplexer to Produce Programmable Gains of 1 to 128

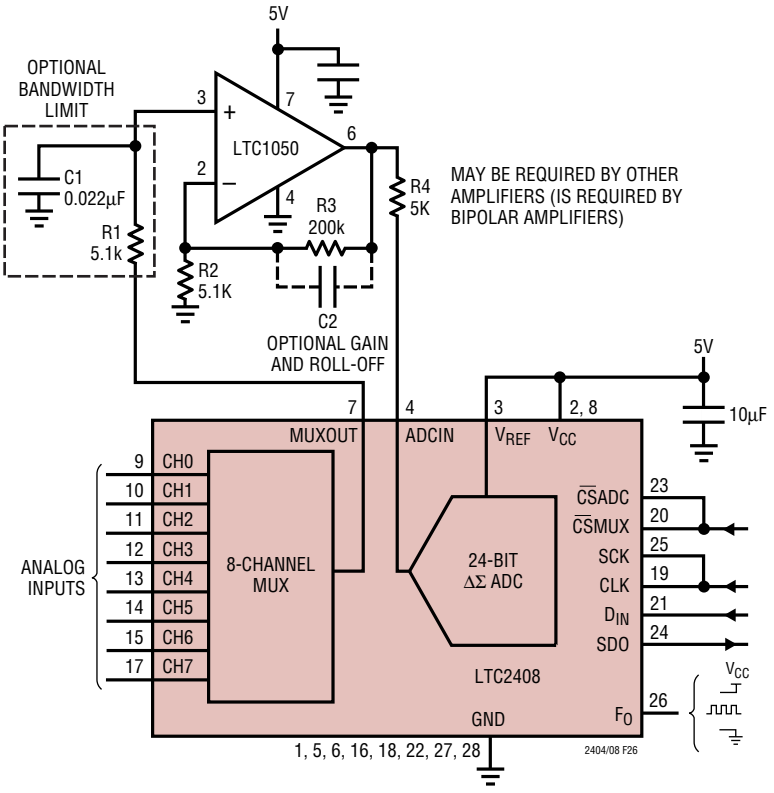

Figure 26. Inserting Gain Between the Multiplexer and the ADC Input

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noise bandwidth of the system to 6Hz. The noise bandwidth of the LTC2408 without any input bandwidth limiting is approximately 150Hz. A roll-off at 1500Hz eliminates all higher order images of the base bandwidth of 6Hz. In the example shown, the optional bandwidth-limiting filter has a –3dB point at 1450Hz. This filter can be inserted after the multiplexer provided that higher source impedance prior to the multiplexer does not reduce the –3dB frequency, extending settling time, and resulting in charge sharing between samples. The settling time of this filter to 20+ bits of accuracy is less than 2ms. In the presence of external wideband noise, this filter reduces the apparent noise by a factor of 5. Note that the noise bandwidth for noise developed in the amplifier is 150Hz. In the example shown, the gain of the amplifier is set to 40, the point at which amplifier noise gain dominates the LTC2408 noise. Input voltage range as shown is then 0V to 125mV DC. The recommended capacitor at C2 for a gain of 40 would be 560pF.

Interfacing the LTC2404/LTC2408 to the 68HC11 Microcontroller

The listing in Figure 28 is a simple assembler routine for the 68HC11 microcontroller. It uses PORT D, configuring it for SPI data transfer between the controller and the LTC2408. The program shows how to select and enable a MUX channel and retrieve conversion data. Figure 27 shows the simple 4-wire SPI connection.

The code begins by declaring variables and allocating four memory locations to store the 32-bit conversion result and a fifth location to store the MUX channel address. This is followed by initializing PORT D's SPI configuration. The program then enters the main sequence. It begins by sending the MUX channel data. It then activates the LTC2408's serial interface by setting the SS output low, sending a logic low to $\overline{CS}$ADC/$\overline{CS}$MUX. This also activates the selected MUX channel. It next waits in a loop for a logic low on the data line, signifying end-of-conversion. After the loop is satisfied, four SPI transfers are completed, retrieving the conversion. The main sequence ends by setting SS high. This places the LTC2408's serial interface in a high impedance state and initiates another conversion. The program in Figure 30 modifies the MUX channel selection routine in Figure 28's listing for selection of 16 channels. Figure 29 shows the connections between the LTC1391, LTC2408 and the 68HC11 controller.

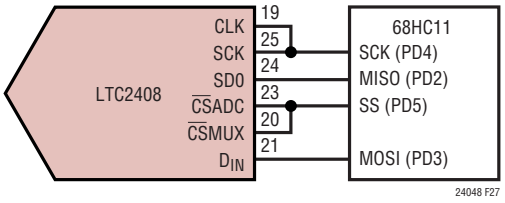

Figure 27. Connecting the LTC2408 to a 68HC11 MCU Using the SPI Serial Interface

```
*********************************************************
*                                                       *
* This example program loads multiplexer channels selection data into  *
* the LTC2408's internal MUX and then transfers the LTC2408's 32-bit  *
* output conversion result to four consecutive 8-bit memory locations.  *
*                                                       *
*********************************************************
*
****************************************
* 68HC11 register definitions                  *
****************************************
*
PORTD   EQU     $1008   Port D data register
*                       " - , - , SS* ,CSK ;MOSI,MISO,TxD ,RxD "
DDRD    EQU     $1009   Port D data direction register
SPCR    EQU     $1028   SPI control register
*                       "SPIE,SPE ,DWOM,MSTR;SPOL,CPHA,SPR1,SPR0"
SPSR    EQU     $1029   SPI status register
*                       "SPIF,WCOL, - ,MODF; - , - , - , - "
SPDR    EQU     $102A   SPI data register; Read-Buffer; Write-Shifter
*
* RAM variables to hold the LTC2408's 32 conversion result
*
```

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```
DIN1    EQU     $00     This memory location holds the LTC2408's bits 31 - 24
DIN2    EQU     $01     This memory location holds the LTC2408's bits 23 - 16
DIN3    EQU     $02     This memory location holds the LTC2408's bits 15 - 08
DIN4    EQU     $03     This memory location holds the LTC2408's bits 07 - 00
MUX     EQU     $04     This memory location holds the MUX address data
*
****************************************
* Start GETDATA Routine                *
****************************************
*
        ORG     $C000   Program start location
*       LDS     $CFFF   Top of C page RAM, beginning location of stack
INIT1   LDAA    #$2F    -,-,1,0;1,1,1,1
*                       -, -, SS*-Hi, SCK-Lo, MOSI-Hi, MISO-Hi, X, X
        STAA    PORTD   Keeps SS* a logic high when DDRD, bit 5 is set
        LDAA    #$38    -,-,1,1;1,0,0,0
        STAA    DDRD    SS* , SCK, MOSI are configured as Outputs
*                       MISO, TxD, RxD  are configured as Inputs
* DDRD's bit 5 is a 1 so that port D's SS* pin is a general output
        LDAA    #$50
        STAA    SPCR    The SPI is configured as Master, CPHA = 0, CPOL = 0
*                       and the clock rate is E/2
*                       (This assumes an E-Clock frequency of 4MHz. For higher
*                       E-Clock frequencies, change the above value of $50 to a
*                       value that ensures the SCK frequency is 2MHz or less.)
GETDATA PSHX
        PSHY
        PSHA
        LDX     #$0     The X register is used as a pointer to the memory
*                       locations that hold the conversion data
        LDY     #$1000
*
*********************************
* The next routine sends data to the   *
* LTC2408 an sets its MUX channel   *
*********************************
*
        LDAA    $MUX    Retrieve MUX address
        ORAA    #$08    Set the MUX's ENABLE bit
        STAA    SPDR    Transfer Accum. A contents to SPI register to initiate
*                       serial transfer
WAITMUX LDAA    SPSR    Get SPI transfer status
        BPL     WAITMUX  If the transfer is not finished, read status
*
****************************************
* Enable the LTC2408                   *
****************************************
*
        BCLR    PORTD,Y %00100000  This sets the SS* output bit to a logic
*                               low, selecting the LTC2408
*
****************************************
* The next short loop waits for the    *
* LTC2408's conversion to finish before *
* starting the SPI data transfer       *
****************************************
*
CONVEND LDAA    PORTD           Retrieve the contents of port D
        ANDA    #%00000100      Look at bit 2
*                               Bit 2 = Hi; the LTC2408's conversion is not
*                               complete
*                               Bit 2 = Lo; the LTC2408's conversion is complete
        BNE     CONVEND         Branch to the loop's beginning while bit 2 remains
*                               high
```

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```
*
****************************************
* The SPI data transfer                *
****************************************
*
TRFLP1  LDAA    #$0         Load accumulator A with a null byte for SPI transfer
        STAA    SPDR        This writes the byte into the SPI data register and
*                           starts the transfer
WAIT1   LDAA    SPSR        This loop waits for the SPI to complete a serial
*                           transfer/exchange by reading the SPI Status Register
        BPL                 WAIT1    The SPIF (SPI transfer complete flag) bit is the SPSR's
*                           MSB and is set to one at the end of an SPI transfer. The
*                           branch will occur while SPIF is a zero.
        LDAA    SPDR        Load accumulator A with the current byte of LTC2408 data
*                           that was just received
        STAA    0,X         Transfer the LTC2408's data to memory
        INX                 Increment the pointer
        CPX                 #DIN4+1 Has the last byte been transferred/exchanged?
        BNE                 TRFLP1 If the last byte has not been reached, then proceed to
*                           the next byte for transfer/exchage
        BSET    PORTD,Y %00100000  This sets the SS* output bit to a logic
*                                  high, de-selecting the LTC2408
        PULA                Restore the A register
        PULY                Restore the Y register
        PULX                Restore the X register
        RTS
```

Figure 28. LTC2408-68HC11 MCU Digital Interface Routine

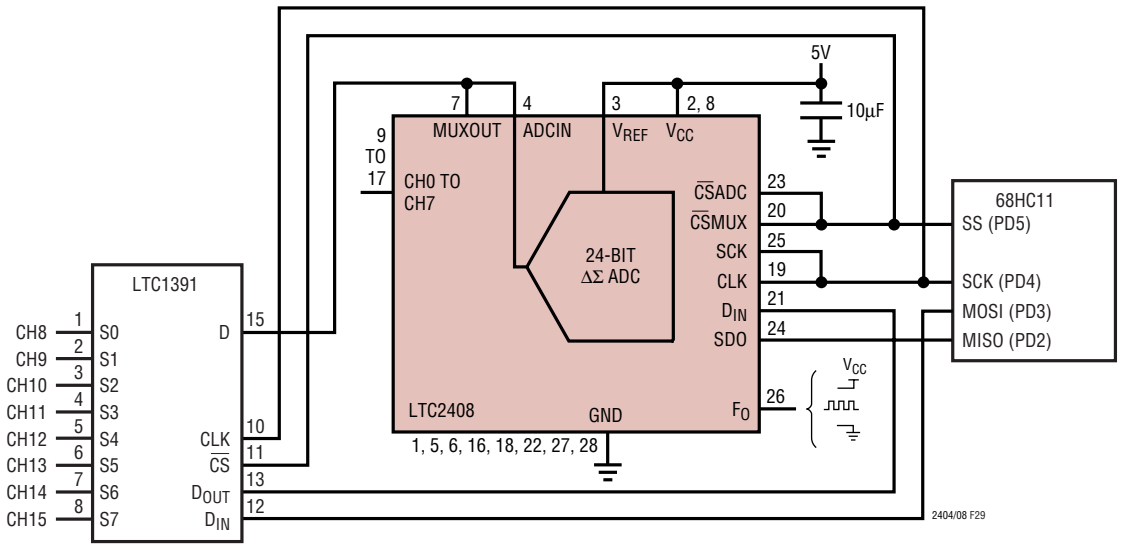

Figure 29. Combining the LTC2408 with the LTC1391 for 16 Input Channels

APPLICATIONS INFORMATION

```
*****************************************************************************
*                                                                           *
* This example program loads multiplexer channels selection data into       *
* either the LTC2408's internal MUX or an external LTC1391 MUX. It then     *
* transfers the LTC2408's 32-bit output conversion result to four           *
* consecutive 8-bit memory locations.                                       *
*
*
*****************************************************************************
*
****************************************
* 68HC11 register definitions          *
****************************************
*
PORTD   EQU     $1008   Port D data register
*                       " -  , -  , SS* ,CSK ;MOSI,MISO,TxD ,RxD "
DDRD    EQU     $1009   Port D data direction register
SPCR    EQU     $1028   SPI control register
*                       "SPIE,SPE ,DWOM,MSTR;SPOL,CPHA,SPR1,SPR0"
SPSR    EQU     $1029   SPI status register
*                       "SPIF,WCOL, -  ,MODF; -  , -  , -  , -  "
SPDR    EQU     $102A   SPI data register; Read-Buffer; Write-Shifter
*
* RAM variables to hold the LTC2408's 32 conversion result
*
DIN1    EQU     $00     This memory location holds the LTC2408's bits 31 - 24
DIN2    EQU     $01     This memory location holds the LTC2408's bits 23 - 16
DIN3    EQU     $02     This memory location holds the LTC2408's bits 15 - 08
DIN4    EQU     $03     This memory location holds the LTC2408's bits 07 - 00
MUX     EQU     $04     This memory location holds the MUX address data
*
****************************************
* Start GETDATA Routine                *
****************************************
*
        ORG     $C000   Program start location
INIT1   LDAA    #$2F    -,-,1,0;1,1,1,1
*                       -, -, SS*-Hi, SCK-Lo, MOSI-Hi, MISO-Hi, X, X
        STAA    PORTD   Keeps SS* a logic high when DDRD, bit 5 is set
        LDAA    #$38    -,-,1,1;1,0,0,0
        STAA    DDRD    SS* , SCK, MOSI are configured as Outputs
*                       MISO, TxD, RxD  are configured as Inputs
* DDRD's bit 5 is a 1 so that port D's SS* pin is a general output
        LDAA    #$50
        STAA    SPCR    The SPI is configured as Master, CPHA = 0, CPOL = 0
*                       and the clock rate is E/2
*                       (This assumes an E-Clock frequency of 4MHz. For higher
*                       E-Clock frequencies, change the above value of $50 to a
*                       value that ensures the SCK frequency is 2MHz or less.)
GETDATA PSHX
        PSHY
        PSHA
        LDX     #$0     The X register is used as a pointer to the memory
*                       locations that hold the conversion data
        LDY     #$1000
*
****************************************
* The next routine sends data to the   *
* LTC2408 an sets its MUX channel      *
****************************************
*
        LDAA    MUX     Retrieve MUX address
        TAB             Save contents of Accum. A
        SUBA    #$07    Is the MUX address in the low nibble
        BLE     ENLWMX  If it is, branch to enable the LTC2408's internal MUX
        TBA             Restore contents of Accum. A
        ORAA    #$80    Enable the LTC1391 external MUX
        BRA     MUXSPI  Go to SPI transfer2400
```

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```
ENLWMX  TBA                 Restore contents of Accum. A
        ORAA    #$08        Set the MUX's ENABLE bit
MUXSPI  STAA    SPDR        Transfer Accum. A contents to SPI register to initiate
*                           serial transfer
WAITMUX LDAA    SPSR        Get SPI transfer status
        BPL     WAITMUX     If the transfer is not finished, read status
*
****************************************
* Enable the LTC2408                   *
****************************************
*
        BCLR    PORTD,Y %00100000  This sets the SS* output bit to a logic
*                                  low, selecting the LTC2408
*
****************************************
* The next short loop waits for the    *
* LTC2408's conversion to finish before*
* starting the SPI data transfer       *
****************************************
*
CONVEND LDAA    PORTD               Retrieve the contents of port D
        ANDA    #%00000100          Look at bit 2
*                                   Bit 2 = Hi; the LTC2408's conversion is not
*                                   complete
*                                   Bit 2 = Lo; the LTC2408's conversion is complete
        BNE     CONVEND             Branch to the loop's beginning while bit 2 remains
*                                   high
*
****************************************
* The SPI data transfer                *
****************************************
*
TRFLP1  LDAA    #$0         Load accumulator A with a null byte for SPI transfer
        STAA    SPDR        This writes the byte into the SPI data register and
*                           starts the transfer
WAIT1   LDAA    SPSR        This loop waits for the SPI to complete a serial
*                           transfer/exchange by reading the SPI Status Register
        BPL                 WAIT1 The SPIF (SPI transfer complete flag) bit is the SPSR's
*                           MSB and is set to one at the end of an SPI transfer. The
*                           branch will occur while SPIF is a zero.
        LDAA    SPDR        Load accumulator A with the current byte of LTC2408 data
*                           that was just received
        STAA    0,X         Transfer the LTC2408's data to memory
        INX                 Increment the pointer
        CPX                 #DIN4+1 Has the last byte been transferred/exchanged?
        BNE                 TRFLP1 If the last byte has not been reached, then proceed to
*                           the next byte for transfer/exchage
        BSET    PORTD,Y %00100000  This sets the SS* output bit to a logic
*                                  high, de-selecting the LTC2408
        PULA                Restore the A register
        PULY                Restore the Y register
        PULX                Restore the X register
        RTS
```

Figure 30. LTC2408/LTC1391-684C11 MCU Digital Interface Routine

An 8-Channel DC-to-Daylight Digitizer

The circuit in Figure 31 shows an example of the LTC2408's flexibility in digitizing a number of real-world physical phenomena—from DC voltages to ultraviolet light. All of the examples implement single-ended signal conditioning. Although differential signal conditioning is a preferred approach in applications where the sensor is a bridge-type, is located some distance from the ADC or operates in a high ambient noise environment, the LTC2408's low power dissipation allows circuit operation in close proximity to the sensor. As a result, conditioning the sensor output can be greatly simplified through the use of single-ended arrangements. In those applications where differential signal conditioning is required, chopper

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amplifier-based or self-contained instrumentation amplifiers (also available from LTC) can be used with the LTC2408.

With the resistor network connected to CH0, the LTC2408 is able to measure DC voltages from 1mV to 1kV in a single range without the need for autoranging. The 990k resistor should be a 1W resistor rated for high voltage operation. Alternatively, the 990k resistor can be replaced with a series connection of several lower cost, lower power metal film resistors.

The circuit connected to CH1 shows an LT1793 FET input operational amplifier used as an electrometer for high impedance, low frequency applications such as measuring pH. The circuit has been configured for a gain of 21; thus, the input signal range is $-15mV \leq V_{IN} \leq 250mV$. An amplifier circuit is necessary in these applications because high output impedance sensors cannot drive switched-capacitor ADCs directly. The LT1793 was chosen for its low input bias current (10pA, max) and low noise ($8nV/\sqrt{Hz}$) performance. As shown, the use of a driven guard (and Teflon™ standoffs) is recommended in high impedance sensor applications; otherwise, PC board surface leakage current effects can degrade results.

The circuit connected to CH2 illustrates a precision half-wave rectifier that uses the LTC2408's internal ΔΣ ADC as an integrator. This circuit can be used to measure 60Hz, 120Hz or from 400Hz to 1kHz with good results. The LTC2408's internal $sinc^4$ filter effectively eliminates any frequency in this range. Above 1kHz, limited amplifier gain-bandwidth product and transient overshoot behavior can combine to degrade performance. The circuit's dynamic range is limited by operational amplifier input offset voltage and the system's overall noise floor. Using an LTC1050 chopper-stabilized operational amplifier with a V_{OS} of 5μV, the dynamic range of this application covers approximately 5 orders of magnitude. The circuit configuration is best implemented with a precision, 3-terminal, 2-resistor 10k network (for example, an IRC PFC-D network) for R6 and R7 to maintain gain and temperature stability. Alternatively, discrete resistors with 0.1% initial tolerance and 5ppm/°C temperature coefficient would also be adequate for most applications.

Two channels (CH3 and CH4) of the LTC2408 are used to accommodate a 3-wire 100Ω, Pt RTD in a unique circuit that allows true RMS/RF signal power measurement from audio to gigahertz (GHz) frequencies. The unique feature of this circuit is that the signal power dissipated in the 50Ω termination in the form of heat is measured by the 100Ω RTD. Two readings are required to compensate for the RTD's lead-wire resistance. The reading on CH4 is multiplied by 2 and subtracted from the reading on CH3 to determine the exact value of the RTD.

While the LTC2408 is capable of measuring signals over a range of six decades, the implementation (mechanical, electrical and thermal) of this technique ultimately determines the performance of the circuit. The thermal resistance of the assembly (the 50Ω/RTD mass to its enclosure) will determine the sensitivity of the circuit. The dynamic range of the circuit will be determined by the maximum temperature the assembly is rated to withstand, approximately 850°C. Details of the implementation are quite involved and are beyond the scope of this document. Please contact LTC directly for a more comprehensive treatment of this implementation.

In the circuit connected to the LTC2408's CH5 input, a thermistor is configured in a half-bridge arrangement that could be used to measure the case temperature of the RTD-based thermal power measurement scheme described previously. In general, thermistors yield very good resolution over a limited temperature range. Measurement resolution of 0.001°C is possible; however, thermistor self-heating effects, thermistor initial tolerance and circuit thermal construction can combine to limit achievable resolution. For the half-bridge arrangement shown, the LTC2408 can measure temperature changes over 5 orders of magnitude.

Connected to the LTC2408's CH6 input, an infrared thermocouple (Omega Engineering OS36-1) can be used in limited range, noncontact temperature measurement applications or applications where high levels of infrared light must be measured. Given the LTC2408's $0.3ppm_{RMS}$ noise performance, measurement resolution using infrared thermocouples is approximately 0.03°C—equivalent to the resolution of a conventional Type J thermocouple.

Teflon is a trademark of Dupont Company.

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These infrared thermocouples are self-contained: 1) they do not require external cold junction compensation; 2) they cannot use conventional open thermocouple detection schemes; and 3) their output impedances are high, approximately 3kΩ. Alternatively, conventional thermocouples can be connected directly to the LTC2408 (not shown) and cold junction compensation can be provided by an external temperature sensor connected to a different channel (see the thermistor circuit on CH5) or by using the LT1025, a monolithic cold-junction compensator IC.

The components connected to CH7 are used to sense daylight or photodiode current with a resolution of 300pA. In the figure, the photodiode is biased in photoconductive mode; however, the LTC2408 can accommodate either photovoltaic or photoconductive configurations.

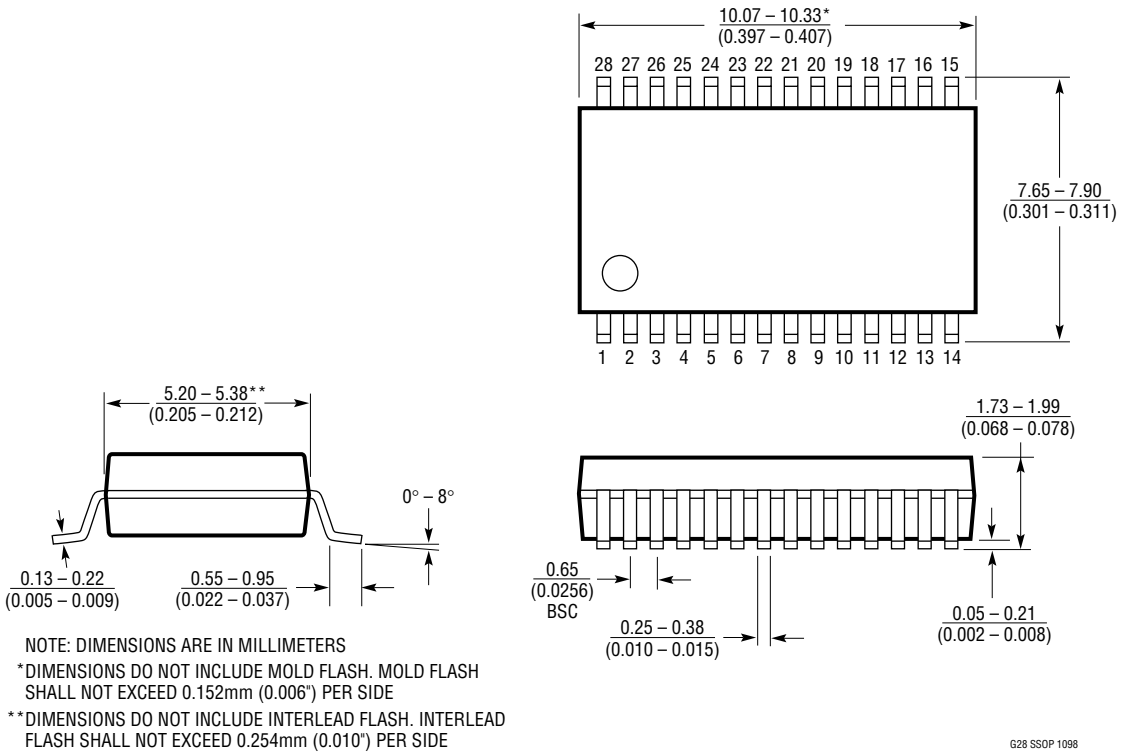
The photodiode chosen (Hammatsu S1336-5BK) produces an output of 500mA per watt of optical illumination. The output of the photodiode is dependent on two factors: active detector area (2.4mm • 2.4mm) and illumination intensity. With the 5k resistor, optical intensities up to 368W/m^2 at 960nM (direct sunlight is approximately 1000W/m^2) can be measured by the LTC2408. With a resolution of 300pA, the optical dynamic range covers 6 orders of magnitude.

The application circuits shown connected to the LTC2408 demonstrate the mix-and-match capabilities of this multiplexed-input, high resolution ΔΣ ADC. Very low level signals and high level signals can be accommodated with a minimum of additional circuitry.

PACKAGE DESCRIPTION

Dimensions in millimeters (inches) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



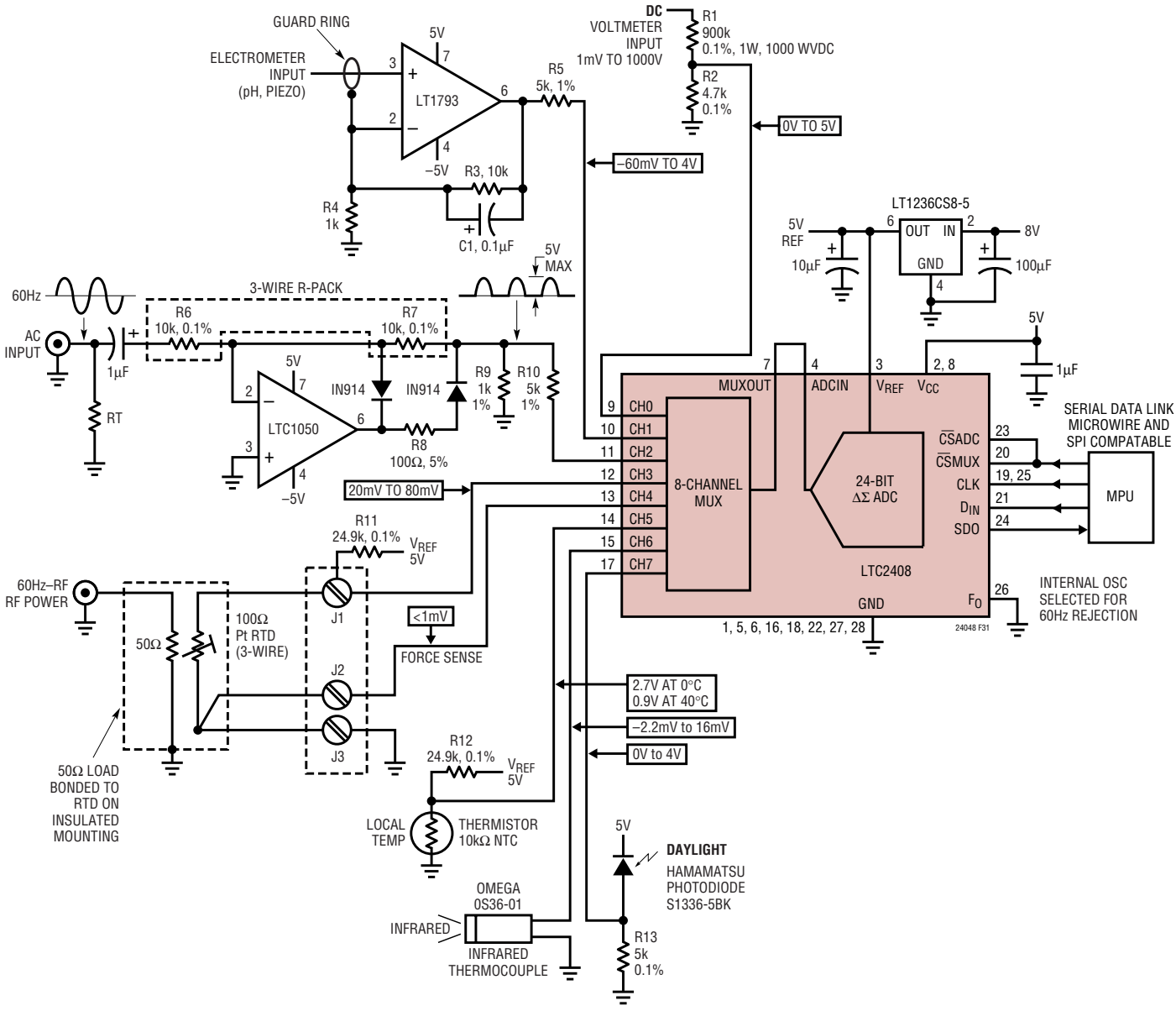
NOTE: DIMENSIONS ARE IN MILLIMETERS

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

G28 SSOP 1098

TYPICAL APPLICATION



Fiugre 31. Measure DC to Daylight Using the LTC2408

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1050	Precision Chopper Stabilized Op Amp	No External Components, 5µV Offset, 1.6µV$_{P-P}$
LT1236	Precision Bandgap Reference	0.05% Max Initial Accuracy, 5ppm/°C Drift
LT1793	Low Noise JFET Input Op Amp	10pA Max Input Bias Current, Low Voltage Noise: 8nV
LTC2400	24-Bit Micropower ΔΣ ADC in SO-8	<4ppm INL, No Missing Codes, 4ppm Full Scale
LTC2424/LTC2428	20-Bit 4-/8-Channel ΔΣ ADCs	1.2ppm Noise, 8ppm INL, Fast Mode

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